THE EFFECTS OF PRIOR NITRIDATION PROCESS OF SILICON SURFACE AND DIFFERENT METAL GATES ON THE CAPACITANCE VOLTAGE CHARACTERISTICS OF METAL-TA_2O_5-SI MOS CAPACITOR

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ABSTRACT

THE EFFECTS OF PRIOR NITRIDATION PROCESS OF SILICON SURFACE AND DIFFERENT METAL GATES ON THE CAPACITANCE VOLTAGE CHARACTERISTICS OF METAL-TA_2O_5-SI MOS CAPACITOR

According to the 2004 International Technology Roadmap of Semiconductor (ITRS), for sub-micron technology, an equivalent oxide thickness (EOT) less than 1 nm is required. However, for such thickness levels, the native oxide SiO_2 is unacceptable since it does not posses its inherited physical properties and results in high leakage current density resulting in reduced device performance. The replacement of SiO_2 with high dielectric constant material (high-k) may eliminate such problems since it will allow the usage of thicker dielectric material. The leakage current will be reduced while maintaining the same levels of inversion charge. In this study, the electrical properties of metal-Ta_2O_5-Si MOS capacitor were investigated for devices prepared with different conditions. A prior nitridation process of silicon surface in N_2O and NH_3 gas before Ta_2O_5 was carried out to improve interface quality. In addition, different metal gates formed on the Ta_2O_5 oxide layer were also used in order to see the effects of top oxide-metal gate on the electrical properties of MOS capacitors. The metal gates used are Al, TiN and W. High frequency (1MHz) Capacitance-Voltage Spectroscopy was used to understand the effects of prior nitridation process and metal gates on the Ta_2O_5 high-k oxide properties. From the analysis of high frequency C-V curves, oxide capacitance, dielectric constant, EOT, leakage current density, conductance, flat band voltage V_{FB} shift, mobile charge density, effective oxide charge and interface trap density D_{it} were obtained and compared with those of reference samples. Reference sample -1 has native oxide SiO_2 and Al metal gate and Reference sample-2 has Ta_2O_5 oxide layer with unnitrided silicon surface.

It has been found that, the replacement of SiO_2 gate oxide with Ta_2O_5 oxide layer results in an increase in dielectric constant by several factors and using nitridation process prior to Ta_2O_5 oxide layer improves the interface properties. Many promising results were obtained for samples with W metal gates and nitrided silicon surface prior to formation of Ta_2O_5 oxide layer. It is potentially applicable to future MOS devices.

ÖZET

METAL-Ta_2O_5-Si MOS KAPASİTÖRLERDE SİLİSYUM YÜZEYİNİN ÖN NİTRÜRLEME İŞLEMİ VE FARKLI METAL KONTAKLARIN KAPASİTE GERİLİM KARAKTERİSTİKLERİNE ETKİLERİ

Yarı iletkenlerin uluslar arası teknoloji (ITRS) haritasının 2004 yılındaki açıklamasına göre, mikron-altı teknoloji için, 1 nm den küçük eşdeğer oksit kalınlığına (EOT) ihtiyaç vardır. Fakat bu kalınlıkta doğal SiO_2 kendi fiziksel özelliklerini koruyamadığından ve cihazın performansını düşüren yüksek akım kaçağına neden olduğundan kullanım için pek uygun değildir. SiO_2' in daha yüksek dielectric sabitine sahip bir yalıtkanla değiştirilmesi yukarıda bahsedilen problemleri azaltırken daha kalın bir oksit tabakasının kullanımını sağlar. Bu da SiO_2 ile aynı terslenim yük tabakasını oluştururken kaçak akımı düşürecektir. Bu çalışmada farklı koşullarda hazırlanmış metal-Ta_2O_5-si MOS kapasitörler incelenmiştir. Ara yüzey özelliklerini iyileştirmek için oksit tabakasının büyütülmesinden önce silisyum yüzeyine N_2O ve NH_3 gaz ortamlarında 700–850 ^oC sıcaklık aralığında ön nitrürleme işlemi uygulanmıştır. Bununa beraber, metalin metal-oksit üst ara yüzeyinde MOS kapasitörlerin elektriksel özellikleri üzerindeki etkisini incelemek üzere farklı metal elektrotlar kullanılmıştır. Kullanılan metal elektrotlar sırasıyla Al, TiN ve W. Kullanılan farklı metallerin ve nitrürleme işleminin MOS kapasitörlerin oksit ve ara yüzey üzerindeki etkilerini incelemek için yüksek frekanslı (1MHz) Kapasitans-Gerilim spektroskopisi kullanılmıştır. Yüksek frekansta ölçülen C-V eğrisinden yararlanarak, oksit kapasitansı, dielektrik sabiti, EOT, kaçak akım yoğunluğu, düz bant gerilimi, histerisis kayması, hareketli tuzak yükleri, etkin oksit yük yoğunluğu ve ara yüzey tuzak yoğunluğunu içeren elektriksel özellikler hesaplanmış ve referans örnekleriyle kıyaslanmıştır. Referans örnek-1, doğal oksit SiO_2 ve Al metal gate içermekte ve Referans örnek-2 Ta_2O_5 oksit ve nitrürlenmemiş silisyum yüzeyi içermektedir.

Sonuç olarak, Ta_2O_5' in SiO_2'in yerine kullanılmasıyla dielektrik sabitinin birkaç kata kadar artığı ve ön nitrürleme işleminin ara yüzeyi daha iyi bir hale getirdiği gözlenmiştir. Tungsten metaline ve Ta_2O_5 oksidin büyütülmesinden önce ön nitrürleme işlemine maruz bırakılmış silisyum yüzeyine sahip örneklerde umut verici sonuçlar bulunmuştur. İleride yapılacak olan MOS cihazlarda kullanılabilir.

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after nitridation process at 850 ^oC in N_2O gas ambient…………………...124

CHAPTER 1

INTRODUCTION

The electronics industry has grown rapidly in the past four decades. In the early 1960's, on a piece of semiconductor putting more than one transistor was thought as the cutting edge. Scientists have spent continuous effort to increase the number of devices on the same chip area and the investigations contributed to the world science as cost reduction in fabrication and improvement in device performance (Wolf 2002). The increase of the number of transistor is best presented with Moore's law, as illustrated in Figure 1 with Intel® processors. Moore's law states that the number of transistor roughly doubles every 18 months resulting in higher performance with lower cost (Moore 1965, WEB_2006). Moore's law has been successfully observed for the past forty years by the semiconductor industry, and still expected to be followed in the coming years. The simple but profound statement of Moore's law is the foundations of semiconductor and computing industries. As it is indicated in Moore's law, in order to achieve 1 G-bit and higher capacity Dynamic Random Access Memories (DRAMs), the number of capacitors inside a chip must be increased resulting in scaling down of memory cell which causes several different problems with the conventionally used gate metal and insulators.

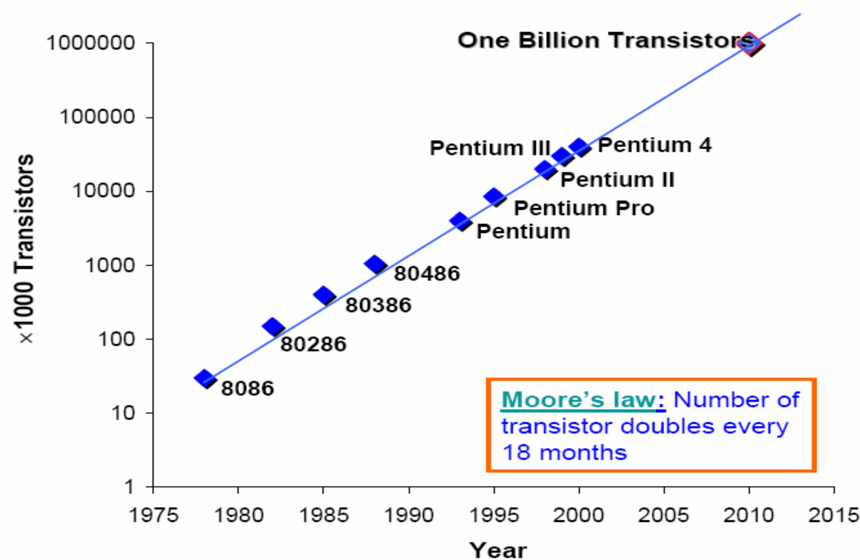


Figure 1.1. Illustration of Moore's law
(WEB_2006)

One of the most crucial elements that allow the successful scaling is certainly the native oxide SiO_2. It is used as a component in Metal- Oxide-Semiconductor (MOS) capacitors of DRAM's, and has served as a high quality electrical insulator for integrated circuit (IC) applications for more than 40 years. SiO_2 passivates Si surface with a low surface-state density which is about 2-3x10^{10}(eV-cm^2)$^{-1}$. Besides its passivating properties, SiO_2 acts as a barrier against the diffusion of impurities into the silicon underneath and insulates the gate from the silicon (Nicollian and Brews 1982). SiO_2 is thermally very stable up to 1000°C which is required for the MOSFET fabrication. In fact, the major driving of the microelectronics revolution is the outstanding properties of SiO_2, which include high resistivity, excellent dielectric strength, a large band gap, a high melting point, and a native, low defect density interface with Si.

In early fabrication technologies, silicon dioxide was frequently used as a mask for ion implantation and than it is usually used for its dielectric properties (Campbell 2001). Since it was the only dielectric material used for the fabrication of integrated circuits it has been studied in detail by many researchers (Nicollian and Brews 1982). In order to achieve devices with best electronic quality, SiO_2 is formed by using various methods such as rapid thermal annealing (Paskaleva et al. 1995) and rapid thermal nitridation (Moslehi et al. 1985). The surface states of silicon-silicon dioxide interface have been extensively investigated by several techniques including measurement of the energy distribution of surface trap states using the high-frequency (Terman 1962) and quasistatic (Berglund 1966, Kuhn 1970) capacitance methods, the conductance method (Nicollian and Goetzberger 1967), and the Gray and Brown technique (Gray and Brown 1966, Brown and Gray 1968). In addition, deep-level transient spectroscopy (DLTS) (Schulz and Johnson 1977, Tredwell and Viswanathan 1980, Nicollian and Brews 1982), 1/f noise measurement (Butler and Hsiang 1988) and charge pumping (CP) measurement techniques (Militaru et al. 2005) have also been used to characterize interface properties.

MOS capacitors are the easiest MOS devices and any further development in these devices can easily be applied to the transistor technology. In a MOS transistor, applying bias to the gate electrode results in an electric field across the transistor structure. This electric field arranges the carrier concentration in the channel and controls the flow of current from the source to drain. Scaling down the device size gives rise to an increase in electric field and therefore the performance of the device could be

enhanced since large electric field increases the drain current, which results in faster switching speeds and lower power dissipation. It provides the consumer with faster circuit performance, reduced energy consumption with longer battery lifetime and reduced cost integrated circuit. In order to meet the demands for improved IC's performance, the microelectronics revolution has continued and the scaling of minimum feature sizes of devices has been the major force of this revolution. For the needs of high density DRAMs, researchers have started to reduce the thickness of the conventional SiO_2 gate dielectrics from hundreds nm to few nm to maintain the high derive current and gate capacitance. Moreover, scaling the thickness of SiO_2 increases the capacitive coupling of the gate to the substrate and decreases the device resistance. Thus, higher doping concentration can be used in the substrate while maintaining a low resistance. The increase in doping concentration increases the barrier height, therefore provide isolation between source and drain when the device is turned off (Packan 1999).

On the other hand, the technical challenge for continuing device scaling down and Moore's law is the scalability of the oxide thickness of MOS devices below 30 nm due to off-state leakage (leakage current). International Technology Roadmap for Semiconductor (ITRS) provides reasonably detailed guide to device scaling requirements to keep the industry on the Moore's law curve alive. Now, according to the 2004 ITRS an equivalent oxide thickness (EOT) less than 0.8 nm is needed in the near feature to allow the continuity of Moore's law (ITRS 2004). However, in the research carried out on SiO_2 film thinner than 1.5 nm, large leakage current higher than 1 Acm^{-2} have been observed (Gou and Ma, 1998). Moreover, Muller et al. studied SiO_2 with thickness ranging from 7 A^o to 15 A^o on Si by using electron energy loss spectroscopy (EELS) and they could obtained the band gap of the oxide only for two monolayer of SiO_2 (Muller et al. 1999). This observation will set a physical limit to SiO_2 around 7-8 A^o since the thickness of each SiO_2 monolayer is about 3,5- 4 A^o. On the other hand, Timp et al. observed reduced drain current which degraded the device performance in small transistor with less than 1.3 nm SiO_2 thicknesses (Timp et al. 1997). It can be inferred from the frame of scaling device size that, drain current increases with decreasing oxide thickness. Below such thickness values the tunneling current increases exponentially with decreasing oxide thickness due to quantum mechanical tunneling. As a result, gate leakage current continuously increases. Although Moore's law could be satisfied at some point, SiO_2 does not possess its inherited physical characteristics beyond such small thickness.

Since SiO_2 with reduced thickness causes high leakage currents, increase in power consumption, intrinsic device reliability, and circuit instabilities, researchers have suggested using a high-permittivity (high-k) gate insulator with similar properties as SiO_2. Because of its high-k, such material will allow the scientist to use physically thicker oxide in order to obtain the same capacitance value as that of conventional SiO_2. This will provide low leakage current with less probability of electrons and holes tunneling trough the dielectric. In order to be used as gate dielectric, the material should meet a set of criteria such as; dielectric constant higher than that of silicon dioxides (k=3.9), thermodynamic stability on silicon, amorphous structure after device integration, low conduction for low leakage (tunneling current less than 10mA/cm^2), low power consumption, high carrier mobility at the dielectric/Si interface, low interface state density (Dit) (~10^{10} cm^{-2} eV^{-1}), high breakdown strength acceptable reliability and large band gap.

Dielectric constant higher than that of SiO_2 is needed, to obtain the same oxide capacitance as SiO_2. Second important requirement is the thermodynamic stability of high-k dielectric with Si surface. If the high-k material thermodynamically unstable on SiO_2, it will react with underlying Si substrate to form an interfacial layer which might degrade the oxide capacitance and interface properties. On the other hand to minimize the reaction of high-k dielectric with Si, high barrier height is needed. High band gap and band offset are also among the requirement since they prevent the free flow from substrate to metal electrode or vice versa. This will eliminate high leakage current and breakdown problem. Furthermore, the high-k dielectric layer should be amorphous after device integration since crystalline structure can results in non uniform oxide layer and leakage path generation which finally results in higher leakage current.

Finally, the replacement of SiO_2 native oxide with high dielectric constant material has become one of the most important issues of microelectronic industry. Considerable researches have been done on material systems such as Al_2O_3, Ta_2O_5, TiO_2, La_2O_3, Y_2O_3, Hf and Zr metal oxides and their silicates (Jeon et al. 2003, Groner et al. 2002, Dimitrova and Atanassova 1998a, Cambell et al. 1997, Miranda et al. 2005, Callegari et al. 2001, Wang et al. 2003, Rhee et al. 2001). Table 1.1 shows the key properties of high k dielectric candidates (Han 2003).

Table 1.1. Key properties of high k dielectric candidates

Materials	Dielect. Constant (k)	Band Gap (eV)
SiO_2	3,9	8,9
Si_3N_4	7	5,1
Al_2O_3	9	8,7
Y_2O_3	15	5,6
La_2O_3	30	4,3
TiO_2	80	3,5
Ta_2O_5	26-35	4,3-5.3
$ZrSiO_4/HfSiO_4$	13-26	5,8
HfO2	25	1,5
ZrO_2	25	3,4

There has been a significant improvement in the field of alternative high-k gate dielectrics. In spite of this improvement, no clear winner has been declared. Due to its high dielectric constant and thermal stabilization on Si, Ta_2O_5 seems to be one of the most appropriate and compatible material for the conventional DRAM process and selected as a promising dielectric material for the near feature. In addition, Ta_2O_5 films show a considerable interest for a range of application, including optical waveguide devices, high temperature resistors, and oxygen sensors. Moreover, due to its potential application as a dielectric film for storage capacitor, high refractive index and adequate breakdown strength (2 to 4.5 MV/cm).

A number of deposition methods have been used to obtain a Ta_2O_5 thin film. Shirinki et al. used LPCVD method to form Ta_2O_5 films on phosphorus doped poly-crystalline silicon film on an n-type silicon substrate (Shinriki et al. 1989). The source of $Ta(OC_2H_5)_5$ was vaporized at relatively low temperature (~120°C) and introduced in to LPCVD furnace by nitrogen carrier gas, together with oxygen gas. This technique allows the deposition of Ta_2O_5 at relatively low temperature and provides high quality thin films. However, SiO_2 and Ta_xO_y interfacial layers generation affect the stability of the film and degrade the dielectric constant of the oxide in the oxide/semiconductor interface (Chaneliere et al. 1998, Alers et al. 1998).

One of the simple deposition methods is oxidation process of Ta_2O_5 thin film on a Si substrate by using the following steps. First, Ta films were deposited on a Si substrate by RF sputtering from Ta target in an Ar atmosphere. Then, Ta films were oxidized in dry O_2 in a standard oxidation furnace (Atanassova 1999). This method has a few drawbacks such as migration of silicon atoms from the substrate into the bulk of the oxide and high interface trap density and formation of SiO_2 interfacial layer.

Another commonly used deposition method of Ta_2O_5 oxide layer is RF sputtering method. In RF sputtering, Ta_2O_5 thin films was deposited by reactive sputtering of tantalum or tantalum oxide target at low pressure using an Ar/O_2 gas mixture as the sputtering gas (Dimitrova and Atanassova 1998b). Deposition of Ta_2O_5 on silicon substrate has been achieved in two ways: the first one is direct sputtering from the Ta_2O_5 target and the second one is the reactive sputtering from Ta target in oxygen atmosphere. The major benefit of this method is that it can be performed at relatively low temperatures (in the range 150-400 ^oC). However, stoichiometry of the oxide layer obtained with this method is rather difficult to control, and the films generally present low density and often shows numerous pinholes. Inspite of these drawbacks, as the sputtering can be suitably controlled, it may potentially offer considerable material flexibility (Chaneliere et al. 1998).

Furthermore, Ta_2O_5 films were also obtained by sol-gel method (Lee et al. 1992). In this method Ta_2O_5 films were deposited by a spin-coating process. Tantalum oxide coating solutions were prepared by hydrolysis of tantalum ethoxide in absolute ethanol. The tantalum ethoxide was dissolved in ethanol. After the solution had been stirred, it was diluted with ethanol and a small amount of water mixture. The mixed solution was catalyzed with glacial acetic acid and stirred for 18 h to form the sol-solution for the preparation of the Ta_2O_5 films. This solution was then dropped onto the substrate surface (Yildirim et al. 2005). Although this method provides low temperature processing, simple and compact equipment and high homogeneity of the deposited films, the layers are mostly porous and contains large amount of CH based species. In addition, other methods such as anodic oxidation, ion assisted deposition, electron-beam evaporation, plasma enhanced CVD (PECVD), electron-beam vapor deposition or a combination various techniques have been developed in order to obtain Ta_2O_5 oxide layer. Even if the deposition method good or bad, the process must be economical and should provide beneficial electronics properties and reliability for the device. However despite the caution have been taken, XPS and high resolution transmission electron

microscopy (HRTEM) results undoubtedly reveal the formation of an ultra thin SiO_x or Ta_xO_y interfacial layer at the Si- Ta_2O_5 interface for most of the deposition technique while the formation of interfacial SiO_2 is obviously an unavoidable process during deposition of the oxide layer.

Structural characterization of Ta_2O_5 generally carried out using Auger electron spectroscopy (AES), X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS) measurement. Theoretical and experimental study of structural properties of Ta_2O_5 reveals that, depending on the growth condition, the film can either be amorphous or crystalline (Kimura et al. 1983). Research have done on Ta_2O_5 thin film obtained by sol-gel method reveals that the as deposited and annealed at 973 ^oC oxide layers are amorphous whereas crystalline orthorhombic phase of Ta_2O_5 was obtained at annealing temperature above 973 ^oC (Lee et al. 1992). On the other hand, XRD result for thermally grown insulator layers and recent research for Ta_2O_5 obtained with different deposition methods shows that the crystallization temperature is range from 873 ^oC to 973 ^oC and it depends on film thickness and amorphous structures of the oxide (Dimitrova et al. 2000, Kimura et al. 1983). Crystalline phase of Ta_2O_5 presents two structures, orthorhombic (β- Ta_2O_5) and the second one is hexagonal (δ- Ta_2O_5) structure. The β- Ta_2O_5 have lattice constants a=511.748 bohrs, b=56.948 bohrs, and c=514.728 bohrs. It has two formula units of Ta_2O_5 with three Ta-O near neighbor distances of 3.492, 3.674, and 3.809 bohrs. The hexagonal structure also contains two formula units of Ta_2O_5 and two Ta-O near neighbor distances of 3.587 and 3.652 bohrs. Its lattice constants are a=513.697 bohrs and c=57.332 bohrs. Encouraging electrical properties have been obtained for amorphous Ta_2O_5 thin film, whereas there are no sufficient studies on crystalline one. It is undesirable feature since it introduces non-uniformity in the range of grain size and results in leakage path generation it is not suggested to be used.

Optical properties of Ta_2O_5 thin film have been investigated using elipsometry and optical transmission measurement. Ta_2O_5 thin film has an increasing refractive index with the increased film thickness (Atanassova and Spassov 1998, Yoon et al. 2004). It was found that, the value of refractive index for thermally grown Ta_2O_5 is n_{eff} =2 for the lowest thickness value and it increase with the increasing thickness up to 100 nm. It then saturates and stays around 2.22 for thickness higher than 100 nm. Similar experimental results were reported for the reactive index of Ta_2O_5 films prepared using different deposition methods (Chen et al. 1997).

The optical band gap of Ta_2O_5 was determined from the optical transmission measurement. The optical band gap was found to be3.75 ± 0.12 eV for Ta_2O_5 deposited by sol-gel dip- and spin-coating deposition techniques (Tepehan et al. 1997). However, it is reported to be 4.2 eV for films made by RF sputtering method (Babeva et al. 2005). These results indicate that, the optical band gap also depends on the deposition conditions and type of deposition methods.

The conduction mechanism and electrical properties, which attract the scientist to use high-k dielectric for the replacement of native oxide SiO_2 in the development of transistor technology, of Ta_2O_5 thin films are obtained from characteristics of MOS structure. For this purpose Capacitance-Voltage (C-V) (Sun and Chen 1996), Current-Voltage (I-V) (Ma 1997) and Conductance-Voltage (Chakraborty et al. 2004) spectroscopies have been used. Applying voltage between metal gate and substrate in a MOS structure provides one to determine the quality of the oxide layer and the quality of the oxide-semiconductor interface. In addition to that, C-V and I-V and G-V spectroscopies are used to investigate the dielectric constant, flat band voltage, hysteresis behavior of the capacitor, the electrically active defects, conduction mechanism in oxide and leakage current characteristics and doping concentration.

The electrical properties of Ta_2O_5 thin film are strongly dependent on the deposition techniques. It was found that the dielectric constant of Ta_2O_5 shows thickness dependence (Atanassova and Spassov 1998). Dielectric constant increases with the increasing thickness. As the deposition temperature or annealing temperature is increased, the dielectric constant can also be increased. On the other hand, crystalline Ta_2O_5 has a higher dielectric constant than the amorphous one. In MOS capacitors, the insulator should have high breakdown strength in order to prevent the charge flow result from high electric field. When the amorphous Ta_2O_5 film crystallizes the breakdown voltage decreases despite its increased dielectric constant (Dimitrova and Atanassova 1998c). As a result, a rush of charge flow will result in and device is broken down. Once this happens the properties of the insulator becomes unpredictable. Furthermore, the crystalline phase of tantalum pentoxide shows an anisotropic character. Depending upon the crystal orientation, the dielectric constant could vary over a wide range, which finally gives rise to uncertainty in the capacitance per unit area when used to make MOS capacitors. Therefore, it could be possible that the dielectric constant of Ta_2O_5 layers used for submicron transistor structures could be different from one transistor to another giving rise to a wide dispersion of device characteristics. Therefore, an

amorphous structure is preferred for microelectronics applications unless the crystal orientation can be controlled in order to obtain the same characteristics from one component to another.

Conduction mechanism of Ta_2O_5 layers have been studied extensively. Two main conduction mechanisms were suggested to explain the current transport in Ta_2O_5 thin film as Schottky emission and Poole-Frenkel effect. Both mechanisms result from the lowering of a Coulombic potential under an applied electric field. The Schottky current is due to electrons which transit above the potential barrier at the surface of metal or semiconductor and dominant at low electric fields below 2.2 MV/cm. On the other hand, the Poole-Frenkel effect involves field enhanced electron emission from Coulombic donor-like centers such as holes from acceptor centers and is dominant at high fields above 2.2 MV/cm (Lee et al. 2001, Ezhilvalavan and Tseng 1999).

Leakage current density strongly influences the electrical properties of Ta_2O_5. As the thickness of the oxide increases leakage current decreases. Leakage current of Ta_2O_5 generally found to be in the range of 10^{-7}-10^{-8}A/cm^2 under an applied electric field up to 3MV cm^{-1} (Chaneliere et al. 1998). Since the thickness of SiO_2 is increased with increasing of Ta_2O_5 thickness, for thicker oxide film (t_{ox}>150nm), SiO_2 dominates on leakage current (Atanassova and Spassov 1998). That is why the range of the leakage current strongly depends on the deposition condition (temperature, pressure, precursor used) and annealing treatments (annealing technique, gasses employed, duration, presence of an interfacial layer).

It is undoubted, SiO_2 greatly responsible for conduction mechanism. On the other hand there are evidences about the electrically active defects which possibly affect the conduction mechanism in the Ta_2O_5-Si system. These defects result in non ideal effect for MOS capacitors. They are occurs due to the deposition method, type of insulator and environmental condition.

There are two types of charge in the insulator/Si layer; interface trap charge and oxide charge. The oxide charge can be collected in three groups as fixed oxide charge, oxide trapped charge and mobile ionic charge. The total of the oxide charges is called as effective charge, Q_{eff}. The effective oxide charge is independent of gate bias, whereas interface charge trap varies with gate bias. Generally in the conduction mechanism of MOS structure Q_{eff} and the density of interface states caused by structural defect and lattice mismatch between Ta_2O_5-Si interfaces, which is represented by $D_{it,}$ takes a great responsibility. For SiO_2 the D_{it} level generally found to be in the range of ~10^{10}

$(eVcm^2)^{-1}$ and the lower of the D_{it}, the better conduction mechanism thus electrical properties, can be obtained since the expected interface is the one which have the less interface trap charge. However when it's compared with SiO_2, Ta_2O_5 has higher interface state density which is in the range of $\sim 10^{12}$ $(eVcm^2)^{-1}$ due to dangling bond or lattice mismatch.

Although Ta_2O_5 film provides high dielectric constant, however it is thermodynamically unstable on silicon substrate due to the formation Ta_xO_y and unavoidable SiO_2 formation. It has relatively high D_{it} level with high leakage current. Quasi-static capacitance measurement of Ta_2O_5 has not been successfully investigated due to the high level of leakage current. In addition, Ta_2O_5 oxide layer in MOS capacitors show high density of effective oxide charge and hysteresis behaviors as the gate voltage is swept from negative to positive and back to negative voltages. Such hysteresis behavior is the cause of mobile trapped charges present in the oxide. In order to improve the bulk and silicon-oxide interface properties of MOS capacitors with high-k insulating layers, several pre and post deposition processes have been applied in production of high quality devices. Such processes are furnace oxidation in O_2 (Spassov et al. 2000), plasma oxidation (Atanassova et al. 2002b), prior rapid thermal nitridation in NO_2 and NH_3 gas (Novkovski et al. 2005) and rapid thermal annealing (Atanassova et al. 2003a). However, the best results were obtained for the samples exposed to rapid thermal nitridation (RTN) treatment before the formation of Ta_2O_5 oxide layers. Formation of silicon oxynitride ($Si0_xN_y$) layer on a silicon substrate prevents the interfacial SiO_2 film growth problem and enhances the properties of the Ta_2O_5-Si interface (Novkovski et al. 2005). It is also desirable to have such an interfacial layer instead of SiO_2 layer, since it has higher dielectric constant than SiO_2. $Si0_xN_y$ layer passivates silicon surface from the oxide layer and thus helps to maintain high channel mobility and prevents the reaction between the oxide and silicon which results in the generation of the interface states (Gusev et al. 1999). Moreover, it provides an increase in band offset, which increases the barrier height and reduces the leakage current. It is concluded that RTN of the Si surface before deposition of Ta_2O_5 is a beneficial method for remarkable improvement of the parameters of the Ta_2O_5/Si system in terms of dielectric constant, leakage currents and the density of interface states (Novkovski et al. 2005, Tay and Hu 2004, Chaneliere et al. 1998).

The use of high-k dielectric materials will allow a significant reduction in equivalent oxide thickness of the gate oxide itself and provide good electrical

characteristics for the MOSFET technology. However scaling down the device size, that is the gate oxide size; affect not only the inherited properties of the gate oxide but also properties of the gate electrode. Therefore replacement of the conventional gate oxide, SiO_2, with a high-k material is not a long term solution since as the high-k material size scaled down the effect of the gate electrode can not be negligible.

Historically, the material used in MOSFET's include a heavily doped polycrystalline silicon (poly-silicon) gate electrode, a silicon dioxide gate dielectric and lightly doped silicon substrate. Poly-silicon offered excellent thermal stability and implemented a self-aligned process. However, as the device is scaled down and the source/drain junction depths get shallower, the thermal budget becomes limited and may cause insufficient dopant activation. The large boron concentration gradient between the heavily doped poly-silicon gate electrode, the undoped oxide and lightly doped silicon channel causes boron to diffuse rapidly trough sub-20 ^{o}A oxide upon thermal annealing and cause to higher concentration of boron in the channel region. This change in channel doping concentration then results in a shift in threshold voltage which affects the device performance in an unacceptable way (Schaeffer III 2004, Brown et al. 2004). On the other hand, it has been shown that as the electric field increase during the device scaling, polysilicon depletion effect becomes an important issue (Lo, Buchanan and Taur 1994). This depletion effect results in discrepancy between the oxide capacitance and measured capacitance. Since the depleted poly-Si gate will be under inversion and adds another capacitance to the device and increases the EOT. Therefore the finite series capacitance of the poly-silicon gate can no longer be neglected since it has a significant impact on the device performance. At that point, replacing the polysilicon metal gate with appropriate one is come to mind. Thus the depletion and penetration effect will be decreased and these will provide extra reduction in gate oxide thickness. On the other hand, when it is compared with polysilicon, Debye length of metals is shorter and thus it has higher carrier concentration and more effective at screening charge. Moreover metal electrodes prevent the band banding and this assists the device performance (Schaeffer III 2004). But in order to be used as a metal gate, the new material should meet some requirement for the replacement of poly-Si gate metal "(Sjöblom, Westlinder and Olsson, 2005), (Westlinder et al. 2004, Lugan et al. 2002) such as stable in contact with gate dielectric, proper work function and high reliability, metal work function should coincide with the valance band edge and

conductance band edge of Si, low charge density at metal gate/dielectric stack, thermodynamic and chemical compatibility with gate dielectric and process integration.

The most effective requirements for the gate material are the work function and interface thermal stability. Therefore requirements for a silicon compatible gate electrode are stringent. The work function of the gate material, defined as the energy needed to remove an electron from the Fermi level to the vacuum level, has to be within a certain range. The currently required work function for p MOS capacitor is 4.25~5.25 eV (Lander et al. 2002) which is around valence band edge of Si (and around conduction band for n-MOS capacitor). Therefore the random dopant placement induced threshold (V_{th}) fluctuation and degradation in channel mobility would be minimized and the device can come to thermal equilibrium condition without deformation.

Depending on the work function, the suitable metals were used in an appropriate condition. There have been some efforts to use a single metal gate electrode with mid-gap workfunction to simplify the fabrication process. Since the nitridation process improves the interface and the oxide properties, metal-nitride layers also take great attention as a technologically important class of materials due to their mechanical properties as well as chemical stability. Alternative solution was carried out by using multilayer which reduce the gate resistance and improve the matching behavior (Nguyen et al. 2005). In this way the work function can be tuned by adding the second layer.

Presently, several metal gates candidates have been investigated which satisfy the requirements such as TiN, W, Al, Mo, InSb, Ti/W, TiN/W, Ta, Au, TaN, TaSiN, Ru, and TiAlN (Lugan et al. 2002, Lander et al. 2002, Khaleque 1995, Nguyen et al. 2005, Yun et al. 2005, Zier et al. 2004). Figure1.2 shows the distribution of the metals over band edge of Si. These studies are motivated by the fact that it is necessary to form a protective layer against oxidation and penetration of contaminants during high temperature treatments after the oxide deposition.

Ec(4.05)

Al(4.08) Ta(4.19) Mo(4.20) Ti(4.33)

Sn(4.42) W(4.52)

Ru(4.71) Rh(4.80) Pb(4.98)

TiN(4.95) Co(4.97)

Ev(5.17)

Ni(5.10) Ir(5.27) Pt(5.34)

Figure 1.2. Work function of metal candidates

Similar to the deposition of the oxide layer, metal gate is also deposited by using different methods such as thermal evaporation (Atanassova et al. 2002b), dc sputtering and rf sputtering (Lander et al. 2002), ALCVD and PVD (Lugan et al.2002), LPCVD (Han et al. 1994, Cao et al. 1998), electron beam evaporation (Nguyen et al. 2005, Lu et al.2005). However the work function of the metal varies with the deposition process. Lugan et al. obtained 5.3 eV work function for ALCVD (atomic layer chemical vapor deposition) deposited TiN metal while 4.8 eV work function was observed for PVD (physical vapor deposition) deposited TiN metal gate. However it's not clear which metal should be used in conjunction, since the underlying dielectric material strongly influences the thermal, chemical and electrical characteristic of the gate metal. Lemme et al. compared Al, TiN and NiAlN as metal electrodes on oxide/Si system and observed encouraging electrical properties for Al on SiO_2 insulator layer while TiN and NiAlN shows better properties on HfO_2 (Lemme et al.).

Al metal gate became the standard metal gate electrode for early MOS devices because of its ease of deposition and etching, its adherence to SiO_2 and Si surfaces, and its immunity to corrosion. However, it can not withstand for higher temperatures needed for deposition and annealing of interlevel dielectric films due to its low melting and alloying temperature. Fillot et al. investigated the stability of a set of metal gate on HfO_2 using X-ray reflectometry. It was observed that non-stoichiometric Al_xO_y or stoichiometric Al_2O_3 layer exist due to the reaction between Al and oxygen (Fillot et al. 2003). However, other metals such as Ni, Pd and Pt on HfO_2 formed stable interface without any interfacial layer. For Al and Ti, these results were also supported by Ko et al. and Atanassova et al (Ko et al. 1998, Atanassova and Paskaleva 2006). Atanassova and Paskaleva investigated the effect of Al, W and TiN metal gate on the characteristics

of Ta_2O_5 gate oxide in terms of leakage current, breakdown field and dielectric constant (Atanassova and Paskaleva 2006). While they observed interaction between the gate metal and oxide for Al and TiN metal which degraded the characteristics of Ta_2O_5, no reaction between W and Ta_2O_5 were observed. Moreover they observed improved leakage current and dielectric constant for the capacitor with W metal gate.

Although TiN metal gate is compatible with low temperature process it shows reaction with the underlying gate oxide as the temperature increased. Kwon et al. formed TiN film on Ta_2O_5 film obtained by LPCVD (Kwon et al. 1996). They studied the thermal degradation of Ta_2O_5 thin film by using XPS. They observed that, TiN metal electrode oxidize for as deposited film and for capacitor exposed to high temperature process (450-850 ^{o}C) with borophosphorus silicate glass (BPSG) reflow process, the oxidation rate of TiN film increase. The effect of this oxidation in Ta_2O_5 observed to cause deterioration and increase in leakage current. On the other hand, Lander et al. reported that the work function of the metal gate electrode has been adjusted by the incorporation of nitrogen at the metal-oxide interface. They observed that the diffused concentration of nitrogen increases with annealing temperature (Lander et al. 2002). Nitrogen diffusion allows high concentration of mobile nitrogen, which greatly influences the effective oxide charge and interface trap charge density in MOS capacitor.

Even though there are several studies reported in the literature for the investigation of the metal gate on high-k oxide layers, there is no conclusive reported yet. Better candidate for replacement of poly-silicon gate in MOS capacitors with high-k oxide layers require more detailed investigation.

1.1 Thesis Objective

The objective of this thesis is to investigate the effects of prior nitridation of silicon surface and different metal gates on the electronic properties of high-k Ta_2O_5 oxide layers and silicon-high-k oxide interface properties. For this reason, a prior nitridation process of silicon surface before formation of Ta2O5 insulating layers were applied using N_2O and NH_3 gas ambients. Substrate temperature was changed between 700 C and 850 C during the nitridation processes. Then, formation of Ta_2O_5 oxide layers were deposited using RF magnetron sputtering of Ta target in Ar and O_2 gas. Finally, Al

metal contacts were evaporated on the high-k Ta_2O_5 oxide. In order to compare the effects of prior nitridation process under two different gas ambients, two different reference samples were also investigated. The first reference sample has the structure of Al-SiO_2-Si MOS capacitor and the second one was Al-Ta_2O_5-Si MOS capacitor without any nitridation process of silicon surface. The high frequency C-V characteristics, G-V, hysteresis C-V, and leakage current measurements were simultaneously performed on several dots from each substrate. By using the theoretical C-V and high frequency experimental C-V curves, effective dielectric constant, doping concentration of Si substrate, flat band voltage shift, effective oxide charge density and finally interface trap density were calculated for the samples. Then the results were compared with those of reference samples. The improvements in the oxide and interface properties with the nitridation process were indicated.

The second objective of this thesis was to investigate the effect of metal gate, which can potentially change the properties of metal gate-oxide interface and finally affects the characteristics of MOS capacitors. Different metal gates such as Al, TiN and W were used as top electrode with Ta_2O_5 high-k oxide layer underneath. The effect of different metal gates with the same oxide layer underneath was compared using the results of high frequency C-V measurements, hysteresis C-V, G-V, and leakage current measurements. Promising gate metal to replace the poly silicon gate contact was determined from the analysis of the results.

CHAPTER 2

EXPERIMENTAL METHODS

2.1. Sample Preparation

Metal-oxide semiconductor MOS capacitors used in this thesis were prepared in five different groups, the first one is in the form of Al-SiO_2-Si and used as Reference sample 1. P-type silicon substrate is used in Reference sample 1. The second one is in the form of Al-Ta_2O_5-Si and used as Reference sample 2. In Reference sample 2, Ta_2O_5 oxide layer was formed using thermal oxidation of thin Ta metal film deposited on p-type silicon substrate using RF magnetron sputtering process. Thermal oxidation process was carried out in dry O_2 atmosphere at 823 K using a standard oxidation furnace. The third group of MOS capacitors is in the form of Al-Ta_2O_5-(SiO_xN_y)-Si, where a prior nitridation process of silicon surface was performed in N_2O and NH_3 gas at temperature between 700 ^oC and 850 ^oC before formation of Ta_2O_5 oxide layers. Rapid thermal nitridation (RTN) process on p-type silicon surface was applied for 10 s in a clean room of class 10 in Germany. The thickness of the silicon oxynitride was around 1.5 nm. Then Ta_2O_5 thin films were deposited using RF magnetron sputtering from Ta target in Ar and O_2 gas environment at substrate temperature of 493 K in Institute of Solid State Physics, Bulgarian Academy of Science, Sofia, Bulgaria. The system base pressure was $6x10^{-4}$ Pa, the working gas pressure 3 Pa, the RF power density 3.6 W/cm^2, the deposition rate, ν = 9 nm/min.

Al gate electrodes in these three groups of sample were finally deposited on SiO_2 and Ta_2O_5 oxide layers using thermal evaporation technique. The gate area of Al electrodes was $1.96x10^{-3}$ cm^2 for Reference sample 1 and varied between $1x10^{-4}$ cm^2 and $2x10^{-3}$ cm^2 for Reference sample 2 and samples in the third group. The structure of the samples and important parameters are also shown in Figure 2.1 and summarized on Table 2.1.

The fourth group of the MOS capacitors was in the form of TiN-Ta_2O_5 (SiO_2)-Silicon. Thermal oxidation process was used to form Ta_2O_5 oxide layer from Ta thin film deposited by RF magnetron sputtering in Ar plasma. Thermal oxidation was carried

out in dry O_2 gas at 823 K. Finally, TiN gate metal was deposited on thermally grown Ta_2O_5 oxide using RF magnetron sputtering technique. During the thermal oxidation of Ta metal films there exists very thin inevitable native oxide SiO_2 between Ta_2O_5 high-k oxide layer and p-type silicon substrate. For this group of samples, a post metallization annealing in H_2 gas was carried out at 450 K for one hour.

The last group of MOS capacitors was prepared in the form of W-Ta_2O_5-SiO_xN_y-Silicon. Similar to the third group samples, a prior nitridation process of p-type silicon substrate was applied in N_2O gas at 700 ^oC and 850 ^oC using RTN process in a clean room of class 10. The thickness of the SiO_xN_y interfacial layer was around 1.5-2 nm. Tantalum films were deposited on Si by RF sputtering of Ta target in Ar atmosphere after the chemical cleaning of the wafer. The system base pressure was $6x10^{-4}$ Pa, the working gas pressure 3 Pa, the RF power density 3.6 W/cm^2, the deposition rate, ν = 9.3 nm/min. During the Ta deposition the substrates were not intentionally heated and presumably remained at a temperature close to the room one. After that, Ta films were oxidized in dry O_2 at atmospheric pressure at 873 K in a standard oxidation furnace. The films thickness were measured as 22 nm by elipsometry (λ = 632.8 nm). The oxidation was fallowed by rf sputtering of W targets to deposit W metal gate on Ta_2O_5 oxide layers. No post metallization annealing was performed.

For all the samples, preparation processes, except RTN process, were carried out by Prof. E. Atanassova at Institute of Solid State Physics, Bulgarian Academy of Science in Sofia, Bulgaria.

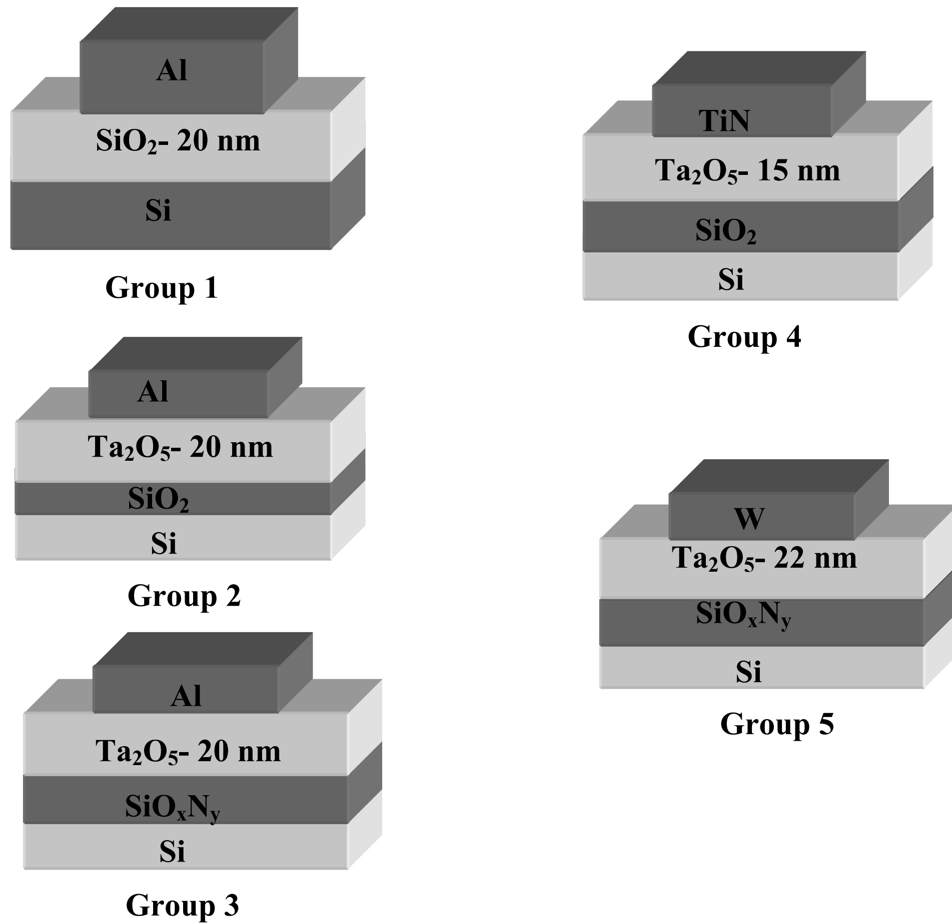


Figure 2.1. Composition of metal-oxide-semiconductor MOS capacitors used in this thesis

Table 2.1. Deposition parameters of MOS structures used in this thesis

Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
Group 1 MOS capacitor- Reference Sample 1						
Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
SiO_2	Al-SiO_2-Si	--------	Thermal in Dry O_2	20	$1.96x10^{-3}$	p-type Si (100) 3-5 Ωcm
Group 1 MOS capacitor- Reference Sample 1						
Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
N6	Al-Ta_2O_5-Si	--------	Thermal in Dry O_2	20	$2.5x10^{-3}$ - $1x10^{-4}$	p-type Si (100) 3-5 Ωcm
Group 3 MOS capacitor						
Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
RN 1	Al-Ta_2O_5-(SiO_xN_y)-Si	N_2O at 700 °C	Reactive sputtering in O_2	20	$2.5x10^{-3}$ - $1x10^{-4}$	p-type Si (100) 3-5 Ωcm
RN 2		N_2O at 800 °C				
RN 3		N_2O at 850 °C				
RN 4		NH_3 at 700 °C				
RN 5		NH_3 at800 °C				
Group 4 MOS capacitor						
Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
N4	TiN-Ta_2O_5-(SiO_2)-Si	-------	Thermal in Dry O_2	15	$2.5x10^{-3}$ - $1x10^{-4}$	p-type Si (100) 15 Ωcm
Group 5 MOS capacitor						
Sample Name	Structure	RTN Process	Oxidation Process	t_{ox} (nm)	Metal Gate Area (cm^2)	Substrate
RN1-T	W- Ta_2O_5-(SiO_xN_y)-Si	N_2O at 700 °C	Thermal in Dry O_2	22	$2.5x10^{-3}$ - $1x10^{-4}$	p-type Si (100) 3-5 Ωcm
RN3-T		N_2O at 850 °C				

2.2 Characterization Techniques

This part will be devoted to the characterization techniques where the instrumentation and details of simultaneous Capacitance- Voltage (C-V) spectroscopy will be given.

2.2.1 Capacitance-Voltage (C- V) Spectroscopy

Model 82-DOS simultaneous C-V spectroscopy is a computer- controlled system of instruments designed to make simultaneous quasistatic C-V and high frequency (100 kHz and 1 MHz) C-V measurements on MOS capacitor. A diagram of the system is shown in Figure 2.2. The system includes Model 590 C-V Analyzer in order to supply high frequency voltage signal and measure capacitance and conductance when making high frequency C-V measurement, and a Model 595 Quasistatic C-V Meter for low frequency C-V and Q/t measurement. In addition, system also includes Model 230-1 DC power supply, which is used to supply a DC voltage of up to ± 100 V and a Model 5951 Remote Input Coupler for connecting the Model 590 and 595 inputs to the device under test. Model 5951 contains tuned circuit which minimizes interaction between low and high frequency measurement. Each instrument is connected to the other by using BNC cables. In order to use the system, the instruments are connected to the computer by using a Keithly IEEE- 488 BUS connection and a model 5957 Software program is used to control the experimental setup and to collect data.

Model 82- DOS system is programmed for Al metal gate and SiO_2 gate oxide on Si substrate. For each MOS capacitor with different oxide layer or metal gate, “Material Constants File”, where the necessary constant and device parameters are stored, should be modified. For every entry to MATERIAL.CON file, even no change have been done, the file should be saved before exiting the file otherwise the program could not locate it at run time. Opening MATERIAL.CON file provides the default menu which as shown in Figure 2.3. For each MOS devices necessary changes were made and the file was saved before exiting the file.

Another important issue is the cable calibration. Since the cables are sensitive to the temperature changes, they should be calibrated frequently. Cable calibration is performed by CABLECAL.EXE utility as shown in Figure 2.4. After running this

utility, the main menu and startup banner will appear on the screen. By pressing the "CONTINUE" button, it is possible to calibrate Model 82-DOS system by entering the "EXECUTE" item. Since each instrument connected to the Model 82-DOS system has a unique address, selecting "Set IEEE Address" will allow to set the IEEE-488 primary addresses for Models 230-1, voltage source, Model 590 C-V analyzer and Model 595 Quasistatic C-V meter as shown in Figure 2.5. The selection of "Cable Cal" Model 82 provides to perform cable calibration of Model 82-DOS system. At the start of the calibration process a window similar to the one shown in Figure 2.6 is displayed. After starting the calibration, the first step is to enter the capacitor values for the Capacitor # 1 and Capacitor # 2, where the value of Capacitor # 1 must be lower than that of Capacitor # 2. Calibration capacitors are supplied with Model 82-DOS. From the window, selecting "OK" completes the entry process. If all the entries are within required limits, the window shown in Figure 2.7 is displayed. From this window selecting "CALIBRATE" starts the complete cable calibration process. After calibration is completed, the new calibration constant must be saved to the PKG82CAL.CAL for the Model 82-DOS. Calibration should be done carefully since failure in calibration will result in substantially reduced accuracy in C-V measurement.

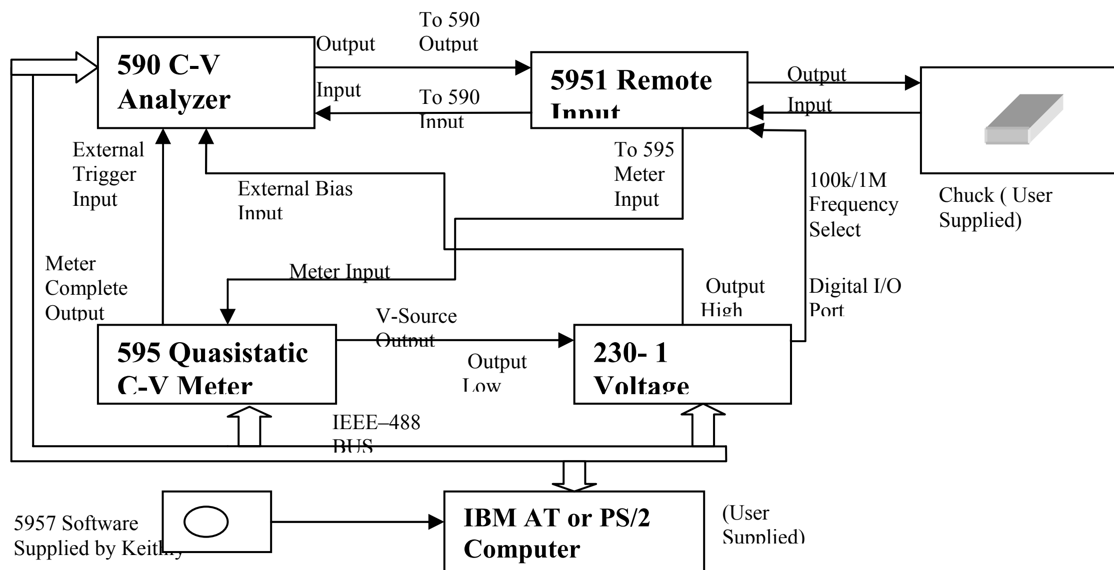


Figure 2.2. Block diagram of simultaneous C-V measurement system used in this thesis

FILE: MATERIAL.CON

DESCRIPTION: This file is used to initialize the physical constants associated with a particular type of MIS device. This file contains physical constants for the following device type at room temperature:

Silicon –Silicon Dioxide – Aluminum

¦ ¦ ¦

¦ insulator ¦

sustrate material ---- gate material ----

VARIABLE	DESCRIPTION	VALUE
KQ	Charge of an electron (Coul)	! = 1.60219E-19
Kk	Boltzmann's constant (J/K)	! = 1.38066E-23
Kt	Test temperature (K)	! = 293
KEox	Permittivity of oxide (F/cm)	! = 3.40000E-13
KEs	Permitivity of semiconductor (F/cm)	! = 1.04000E-12
KEg	Energy gap of semiconductor (eV)	! = 1.12
KNi	Intrinsic carrier concentration (1/cm^3)	! = 1.45000E+10
KPhim	Metal work function (V)	! = 4.1
*KX	Semiconductor electron affinity (V) (see note)	! = 4.15

In modern integrated-circuit processing, heavily doped polysilicon is often used as the gate material instead of aluminum. If this is the case, the work function constants are computed as fallows (as per Sze's book "Physics of Semiconductor Devices").

p-type polysilicon gate

KPhim = Semiconductor electron affinity + Energy gap of semiconductor

n-type polysilicon gate

KPhim = Semiconductor electron affinity

Figure 2.3. Default values stored in material constant

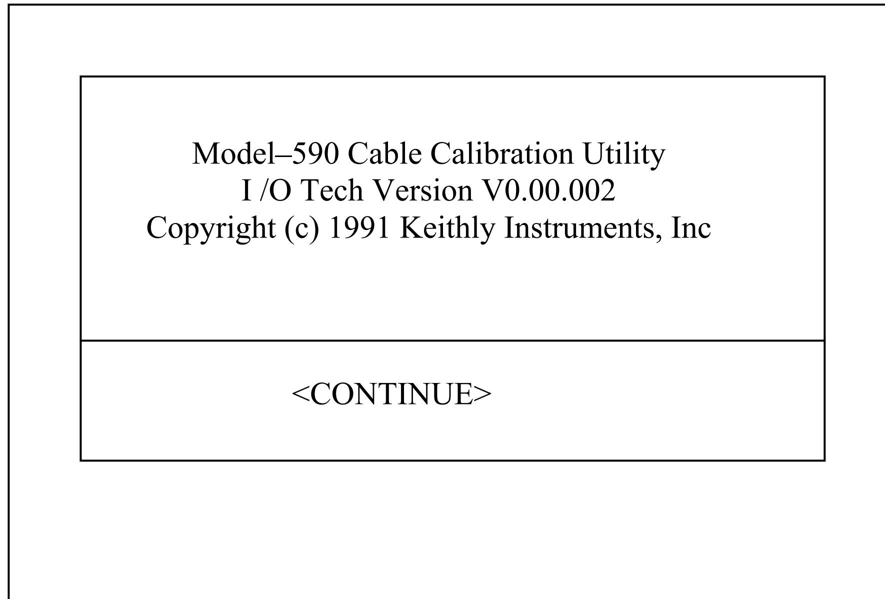


Figure 2.4. Main menu and startup banner

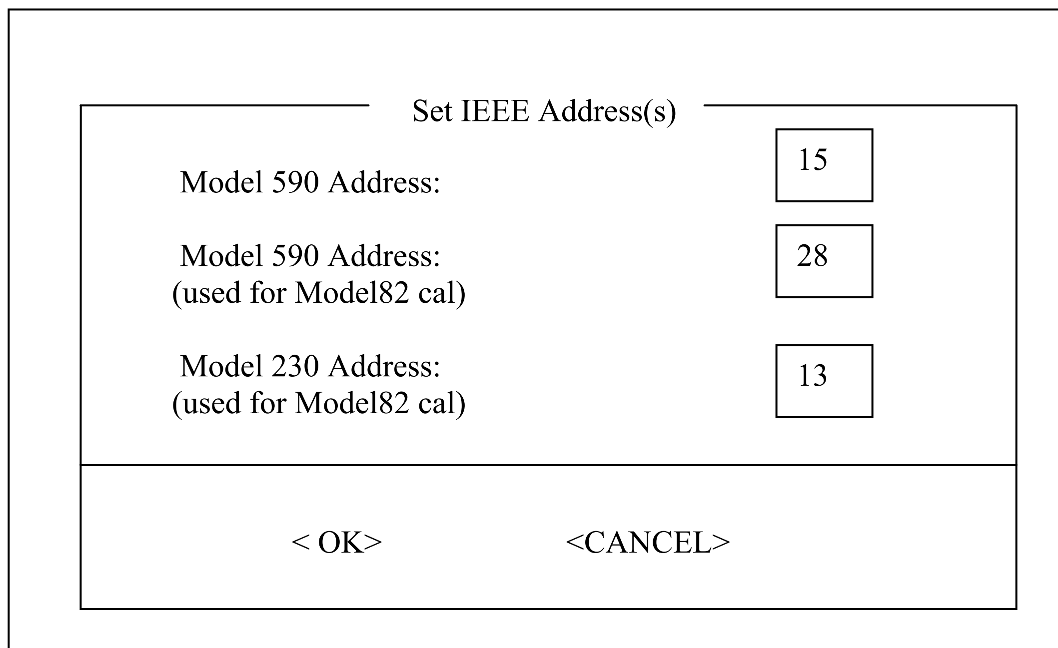


Figure2.5. Set IEEE address window

Model 82: 200 pF Range

CAPACITOR # 1

Nominal	1 kHz	100 kHz	1 MHz
47 pF	46.3864 pF	46.381 pF	46.385 pF

CAPACITOR # 2

Nominal	1 kHz	100 kHz	1 MHz
180 pF	182.732 pF	182.71 pF	182.77 pF

< OK> <CANCEL>

Figure 2.6. Model 82 calibration source value entry window

How do you wish to proceed?

<CALIBRATE> <SEND CONSTANTS> <CANCEL>

Figure 2.7. Calibrate/ Send constants window

After all necessary calibrations and constants modification carried out, for the characterization the sample is placed in a homemade Faraday cage which is made up of aluminum metal. Faraday cage is an enclosure box designed to exclude the effect of electromagnetic fields. The connection of the system to the sample is provided by a homemade probe station with a micro manipulator. Gold wire is used as a probe wire in order to have a good contact the device. To be able to use it as a probe wire, gold wire was first sharpened by the electrolysis process then sanding process was applied to obtain a precise contact area for the smaller gate areas. The contacts are placed on the sample under the optical microscope.

In order to obtain an appropriate start and stop voltage necessary for obtaining the device parameter, a diagnostic C-V measurement should be run from accumulation to the inversion. From the main menu shown in Figure 2.8, option 3 allows us to reach the sub menu for diagnostic C-V measurement as shown in figure 2.9. Before running a sweep, the most important step is to set the start and stop voltages, step voltage and delay time by selecting option 1 in Figure 2.9. Measurement parameters list is shown in figure 2.10.

After setting the parameter list, it is possible to run a diagnostic C-V measurement by selecting option 2 in Figure 2.9. After the measurement is completed, the graph of the measurement can be seen by selecting option 3. A typical graph of C-V measurement is shown in Figure 2.11. If the curve has the expected shape then the device should be biased in accumulation and inversion to determine the oxide capacitance, gate area, oxide thickness, minimum capacitance and optimum delay time as well as series resistance by selecting option 4 and 5 of the menu shown in figure 2.9.

Once the device parameters are obtained, it is possible to run a real C-V measurement by selecting option 4 of the menu shown in Figure 2.8. A sub menu for C-V measurement is shown in Figure 2.12. Selecting “option 1” in Figure 2.12 provides accessing the parameter list. In this menu the step voltage can be selected as small as possible in order to obtain more data points for the accuracy of the analysis. Selecting “option 2” in Figure 2.12 provides making C-V measurement manually. After the measurement is completed option 4 in figure 2.12 is used to analyze the measurement data as shown in Figure 2.13. This menu also provides graphing of the array data.

```
--------------------------------------------------
Keithley Capacitance Measurement System
(c) copyright Keithley Instruments 1991

            Version V2.0
--------------------------------------------------
         ** MODEL 82 MAIN MENU **

1. Reset Model 82 CV System

2. Test and Correct for System Leakages and Strays

3. Compensate for R_series and Determine Device Parameters

4. Make CV Measurements

5. Analyze CV Data

6. Return to DOS


NOTE: ESC always returns user back one MENU level
```

Figure 2.8. Model 82 main menu

```
   ** Characterization of Device Parameters **

   OPEN CIRCUIT SUPPRESS SHOULD PRECEDE EACH MEASUREMENT

1. Set Measurement Parameters

2. Run Diagnostic CV Sweep

3. Graph Diagnostic Sweep Data to Determine INVERSION &

ACCUMULATION Voltages.

4. ACCUMULATION: Determine Rseries, Cox, Tox, and/or Area.

5. INVERSION: Determine Cmin and Equilibrium Delay Time.

6. Return to Main Menu

Enter number to select from menu
```

Figure 2.9. Device characterization menu

** Measurement Parameter List **

Range:	2	Enter R1 for 200pF, R2 for 2nF
Freq :	2	Enter F1 for 100KHZ, F2 for 1MHZ
Model:	1	Enter M1 for parallel, M2 for series
Start V:	2.00 V.	Enter An, -120 <= n <= 120
Stop V:	-2.00 V.	Enter On, -120 <= n <= 120
Bias V:	0.00 V.	Enter Bn, -120 <= n <= 120
TDelay:	0.07 sec.	Enter Tn, 0.07 <= n <= 199.99
Step V:	20 mV.	Enter S10, S20, S50 or S100
CCap:	1	Enter C1 for leakage correction off, C2 for on
Filter:	2	Enter I1 for filter off, I2 for on

Number of samples = 93 Sweep will take = 0.4 minutes.

NOTE: 1) Keep start V and stop V within 40 volts of each other.

2) Keep number of samples within 4 and 1000 points with filter off.

3) Keep number of samples within 50 and 1000 points with filter on

Enter changes one changes at a time. Enter E when done, * for files.

Enter selection:

Figure 2.10. Parameter selection menu

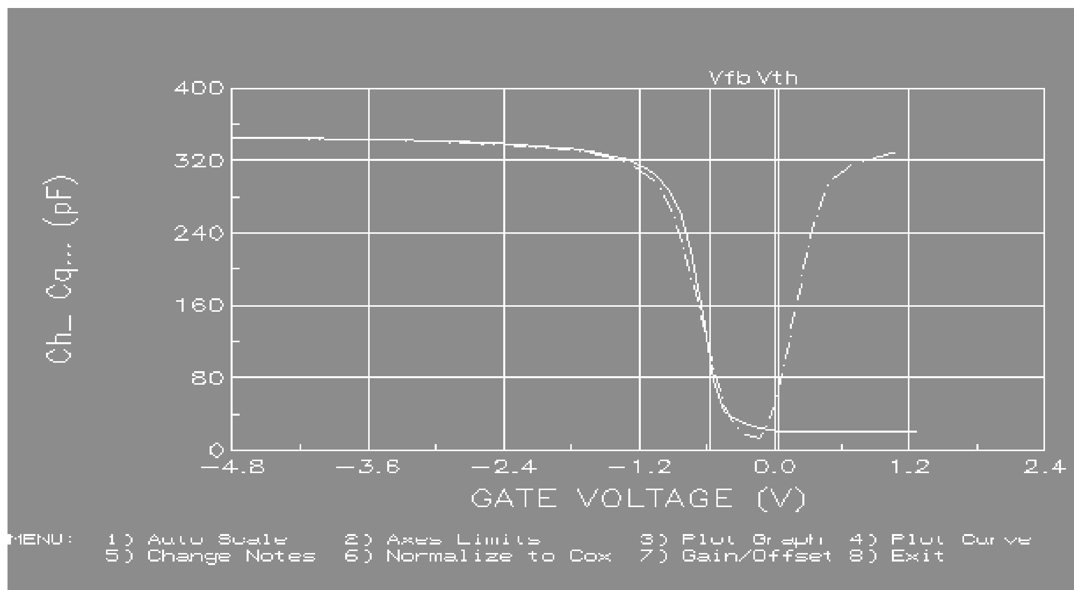


Figure 2.11. High and low frequency C-V graphic of MOS capacitor

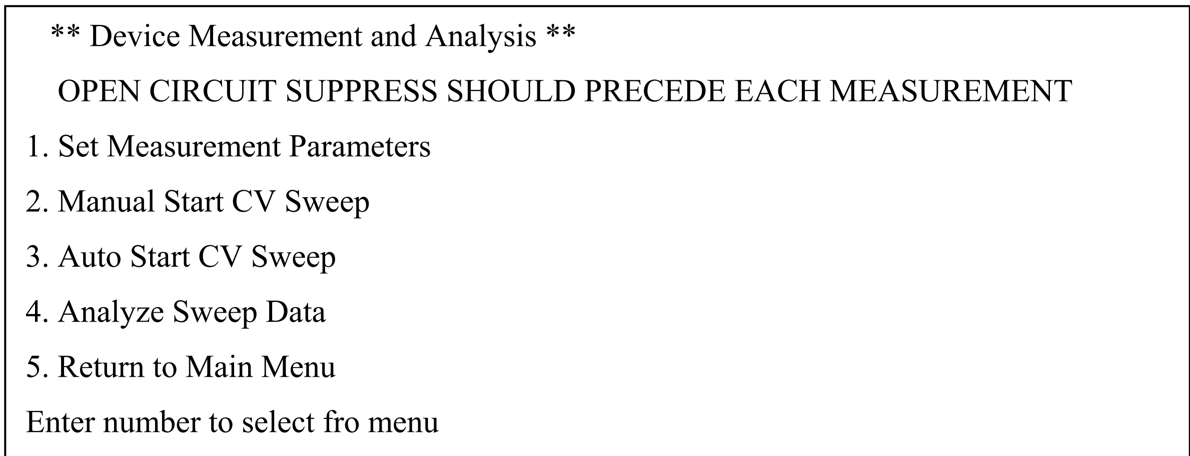

** Device Measurement and Analysis **
OPEN CIRCUIT SUPPRESS SHOULD PRECEDE EACH MEASUREMENT
1. Set Measurement Parameters
2. Manual Start CV Sweep
3. Auto Start CV Sweep
4. Analyze Sweep Data
5. Return to Main Menu
Enter number to select fro menu

Figure 2.12. Device measurement and analysis menu

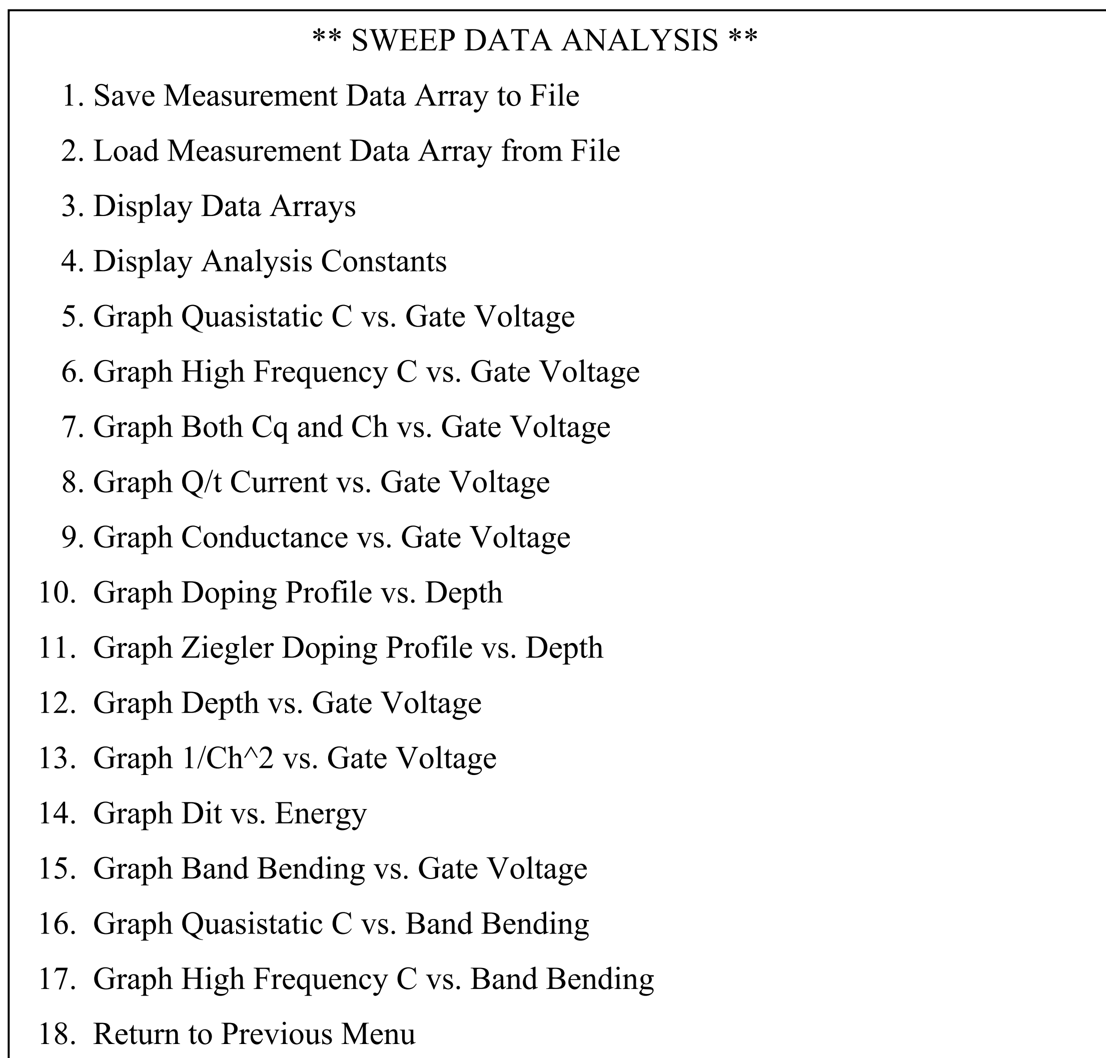

** SWEEP DATA ANALYSIS **
1. Save Measurement Data Array to File
2. Load Measurement Data Array from File
3. Display Data Arrays
4. Display Analysis Constants
5. Graph Quasistatic C vs. Gate Voltage
6. Graph High Frequency C vs. Gate Voltage
7. Graph Both Cq and Ch vs. Gate Voltage
8. Graph Q/t Current vs. Gate Voltage
9. Graph Conductance vs. Gate Voltage
10. Graph Doping Profile vs. Depth
11. Graph Ziegler Doping Profile vs. Depth
12. Graph Depth vs. Gate Voltage
13. Graph 1/Ch^2 vs. Gate Voltage
14. Graph Dit vs. Energy
15. Graph Band Bending vs. Gate Voltage
16. Graph Quasistatic C vs. Band Bending
17. Graph High Frequency C vs. Band Bending
18. Return to Previous Menu

Figure 2.13. Data analysis menu

The "ANALYSIS" menu provides saving, loading and graphing of the reading and graphics array data. It is also provides graphical and mathematical analysis of the data array. In this menu, mathematical analysis of some parameters such as density of interface trap, D_{it}, base on the data array of both high and low frequency C-V measurement are carried out. MOS capacitors are charged by the displacement current induced by the voltage ramp. In order to be able to measure low frequency C-V curve the leakage current through the gate dielectric layer should be negligible compared to displacement current. Although for thick gate oxide this could be obtained, very large tunneling current from thin gate oxide makes the measurement invalid. Since the samples that are used in this study are very thin, only Terman's method is used for MOS devices with Ta_2O_5 oxide layers instead of High-Low frequency C-V method to calculate D_{it}.

The dielectric constant (k), equivalent oxide thickness (t_{eqq}) and flat band (V_{FB}) voltage were calculated by using high frequency C-V curve. The depletion capacitance is used to estimate the Si substrate doping concentration (N). The flat band obtained from the C-V curve was used to calculate effective oxide charge density (Neff). Corrected conductance and leakage current were calculated from the row data of high frequency C-V and conductance. Mobile charge trap obtained from the hysteresis shift, the voltage shift between the reverse and forward bias C-V measurement. Theoretical ideal C-V characteristics were calculated by using a computer program and equation defined for MOS devices. The density of interface trap states were calculated from the high frequency C-V curve by using Terman's method.

CHAPTER 3

PHYSICS OF MOS CAPACITORS AND ANALYSIS

3.1 Ideal MOS Capacitor

The development of MOS technology opened a new path to the development of the commercial devices. Studying this system provides improvement in the performance and stability to the devices such as MOSFET used in integrated circuit. The MOS capacitor is useful in such studies since any change in processing which improves the electrical properties of the MOS capacitor makes the same improvement on the actual devices. In this case understanding of the electrical properties of MOS devices is an important issue.

MOS capacitor is constructed using p or n type crystalline semiconductor wafer. An oxide layer is formed by using different method and finally a metal electrode is evaporated to complete MOS fabrication. A schematic representation of MOS capacitor is shown in Figure 3.1. As represented in this figure, t_{ox} is the thickness of the oxide layer; V_G is the applied voltage on the metal gate electrode. Here, oxide on semiconductor substrate provides protection to the surface, and the interface and the oxide are considered to be ideal and free of charge. The bias voltage V_G is positive when the metal gate is connected to the positive terminal of the bias voltage, and V_G is negative when the metal gate connected to the negative terminal of the bias voltage.

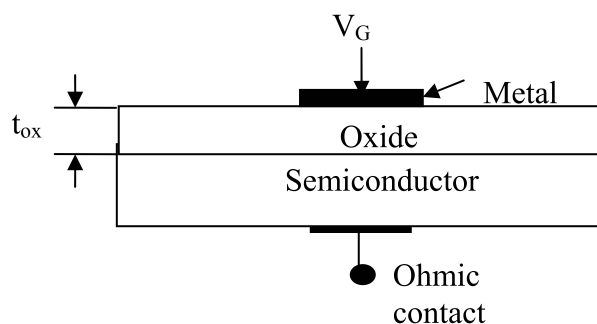


Figure 3.1. Structure of an MOS capacitor.

The detailed analysis of the MOS capacitor begins with the thermal equilibrium band diagram, when the bias voltage $V_G = 0$. The state of thermal equilibrium is defined as the state of an isolated system in which there is no tendency of its macroscopic properties to change with time.

At this state, the Fermi level in the metal and semiconductor must be equal and the vacuum level must be continuous. These two requirements determine a unique energy band diagram for the ideal MOS capacitor. Figure 3.2 shows the energy band diagram of a MOS structure with a p-type substrate. In the figure, ϕ_m is the metal work function χ_i is the electron affinity of the insulator,χ is the electron affinity of semiconductor, E_g is the energy gap of semiconductor, ϕ_B is the potential difference between the metal Fermi level and conduction band of the insulator, ψ_B is the potential difference between the intrinsic Fermi level (E_i) and Fermi level (E_F) inside the bulk, E_C is the conduction band and E_V is the valance band of the semiconductor. The importance of these energy barriers is that they prevent the free flow of carriers from the metal to the silicon or vice versa.

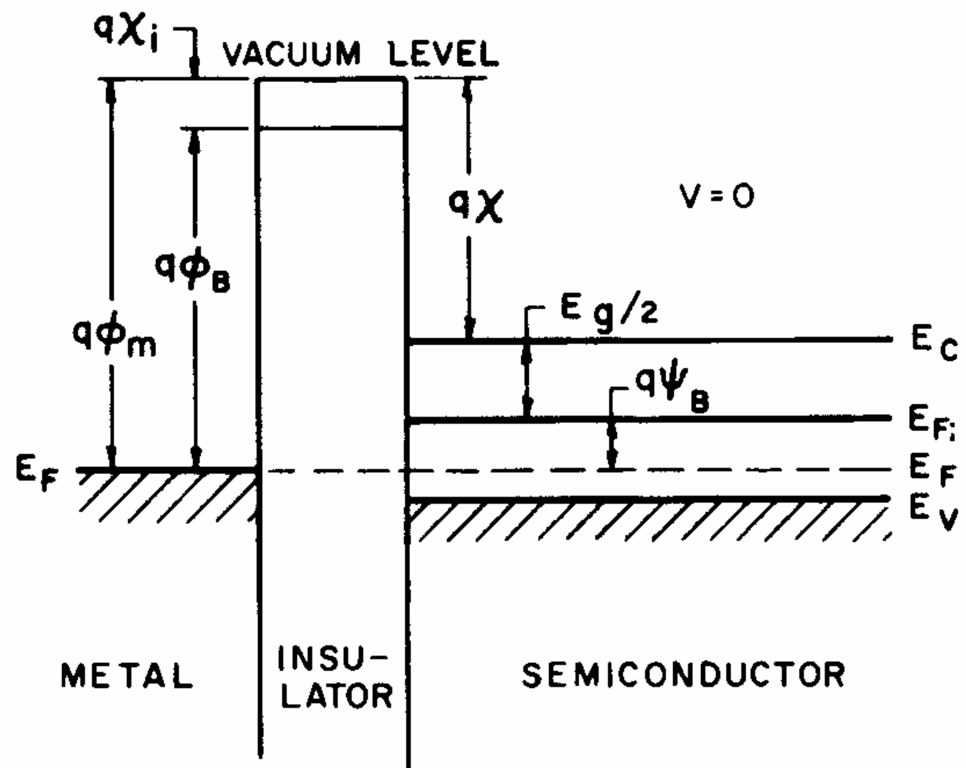


Figure 3.2. Energy-band diagrams for a p-type MOS capacitor at thermal equilibrium.

Depending on the applied voltage band bending occurs and the basic behavior of the capacitor can be seen. When the applied voltage V_G is equal to zero then flat band

which means that the work function difference ϕ_{ms} between the metal electrode work function ϕ_m and the semiconductor work function ϕ_s is equal to zero, occurs. The flat band voltage is the voltage at which there is no charge on the plates of the capacitor and hence there is no electric field across the oxide. Thus when the flat band voltage is applied to the MOS capacitor, the difference in the work function is exactly compensated and the energy bands do not vary with distance. The work function differences in Figure 3.2 for a p-type semiconductor can be written as fallow;

$$\Phi_{ms} = \Phi_m - \Phi_s = \Phi_m - (\chi + \frac{E}{2q} \pm \psi_B) = 0 \tag{3.1}$$

The sign of ψ_B is important since negative sign correlates with n-type semiconductor and positive sign correlates with p-type semiconductor. When the applied voltage $V_G \neq 0$, the charges are distributed at the semiconductor-insulator and metal-insulator interface with equal amount but opposite polarities. At that point, mainly three working conditions present in the semiconductor.

Accumulation: When $V_G<0$ gate voltage is applied to the metal part of a MOS capacitor with p-type semiconductor then the metal part becomes negatively charged while semiconductor part becomes positively charged. An electric field occurs in the direction from semiconductor to the metal. The holes are accelerated upwards and electrons accelerated downwards, inside p-type Si. As a result the holes concentration at the surface will be greater than the holes concentration inside the bulk of semiconductor. In order to preserve the charge neutrality at the surface, the conduction band edge, valence band edge, and intrinsic Fermi level (E_C, E_V, and E_i) near the surface bend upward, which leads to an increase in hole concentration near the oxide semiconductor interface. On the other hand, since there is no electron flow from the metal part to semiconductor or vice versa, Fermi level of the semiconductor does not change. The range of applied gate voltage V_G is called accumulation region" and corresponding of energy band is shown in Figure 3.3.

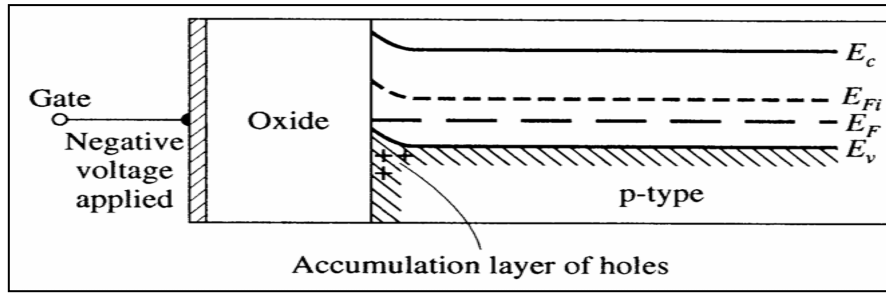


Figure 3.3. Energy band diagram of MOS capacitor in accumulation region.

Depletion: When $V_G>0$ gate voltage is applied to the metal part of a MOS capacitor with p-type semiconductor, the metal part becomes positively charged while semiconductor part becomes negatively charged. Then an electric field is established in the direction from metal to the semiconductor. Majority carrier holes are accelerated toward bulk of semiconductor and electrons are accelerated toward oxide. At this region while the holes pushed away from the interface, a negative space charge region is created at oxide-semiconductor interface due to ionized acceptors. The conduction and valence bands bend downward. The resulting energy-band diagram of the MOS capacitor is shown in Figure 3.4. At the oxide and semiconductor interface the conduction band and intrinsic Fermi levels move closer to the Fermi level. In a distance χ_d from oxide-semiconductor interface towards the bulk of p-type silicon there exist a region where majority carrier hole concentration is less than that of bulk value. For this reason, this region called as “depletion” region.

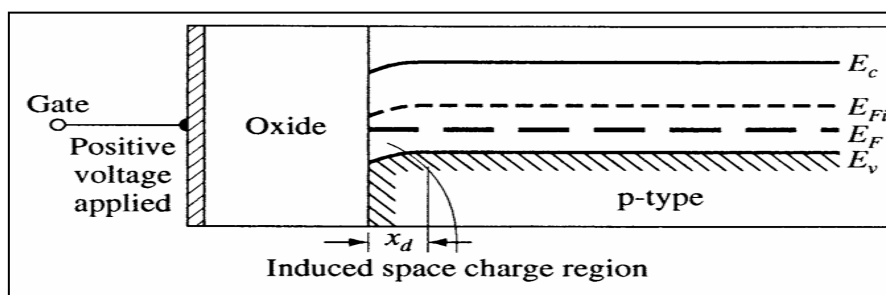


Figure 3.4 Energy band diagram of MOS capacitor in depletion region.

As the applied voltage to the top metal gate of MOS capacitor increases a larger space charge region with more band bending can be obtained. Figure 3.5 shows the energy band diagram of this case. In such case, the Fermi level at the surface is equal to the intrinsic level while it is below the intrinsic level in the bulk semiconductor. Here

the electron concentration at the surface is equal to the hole concentration in the neutral bulk semiconductor. This condition is known as the threshold inversion point. The applied gate voltage at this condition is known as the threshold voltage, V_{TH}. Threshold voltage is the gate voltage which gives rise to surface potential $\psi_s = 2\psi_B$. The bulk potential, ψ_B, is defined to be the difference between the Fermi level E_F and intrinsic Fermi level inside the bulk E_{Fi} and is given by

$$\psi_B = \frac{E_F - E_{Fi}}{q} = \frac{kT}{q}.\ln(\frac{N_A}{n_i}) \tag{3.2}$$

where N_A is the acceptor doping concentration and n_i is the intrinsic carrier concentration.

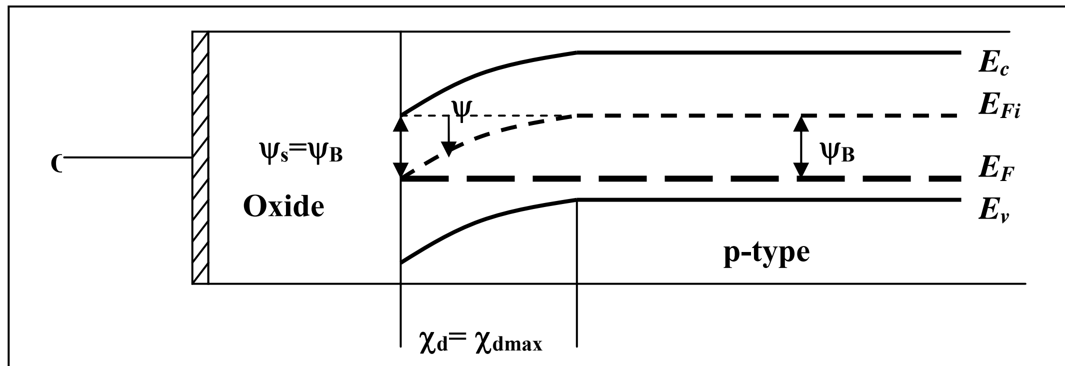


Figure 3.5. Energy band diagram of MOS capacitor at the threshold point.

At threshold voltage V_{TH}, the depletion region thickness x_d reaches its maximum value (x_{dmax}). Further increase in V_G will induce the inversion layer rather than increasing x_d. The potential ψ is defined to be zero in the bulk of the semiconductor. It is measured at the semiconductor surface with respect to the level of E_{Fi} in the bulk of semiconductor as shown in Figure 3.5. For a p-type semiconductor, the electron and hole concentration as a function of ψ are given by the following relation:

$$p_p = p_{po}\exp(-\beta\psi)$$
$$n_p = n_{po}\exp(\beta\psi) \tag{3.3}$$

where n_{po} and p_{po} are the equilibrium densities of electrons and holes respectively in the bulk of semiconductor and $\beta \equiv q/kT$.

3. Inversion: As the applied gate voltage V_G is increased beyond V_{TH} towards positive voltage, the electric field increases and consequently the corresponding positive and negative charges on the MOS capacitors also increases. A larger negative charge on the oxide-semiconductor interface will result in more band bending. In this case, the electron concentration at the surface of semiconductor is greater than the hole concentration in the neutral bulk. This result implies that the surface of the semiconductor is inverted and behaves as if an n-type semiconductor. In the case of inversion, the band diagram of MOS structure is shown in Figure 3.6. At this condition the intrinsic Fermi level at the surface is below the Fermi level, and the conduction band is closer to the Fermi level than the valence band is.

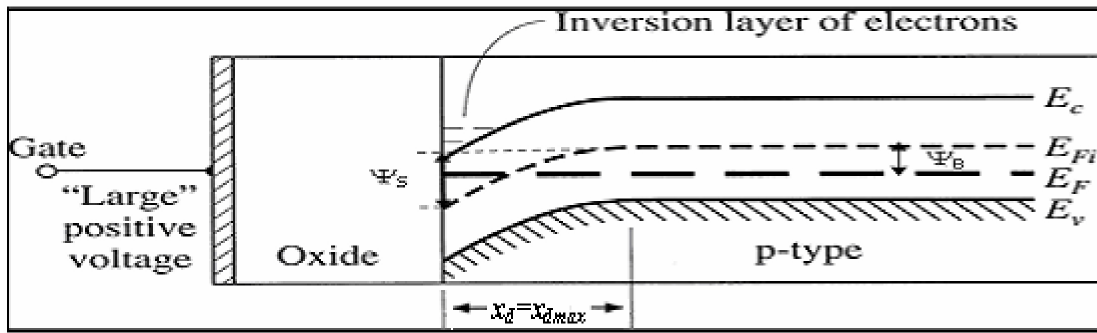


Figure 3.6. Energy band diagram of MOS capacitor in the inversion region.

From the foregoing, it can be concluded that the position of the conduction band, valence band and intrinsic Fermi level is a function of applied gate voltage, V_G. Depending on V_G, surface potential change and this strongly influence the characteristic of the MOS structure. At the semiconductor surface, $\psi=\psi_s$ and ψ_s is called the surface potential which is the difference between E_{Fi} measured in the bulk semiconductor and E_{Fi} measured at the surface. The hole and electron concentration at the surface can be written as

$$p_s = p_{po}\exp(-\beta\psi_s)$$
$$n_s = n_{po}\exp(\beta\psi_s) \qquad (3.4)$$

then using the value of ψ_s, different condition can be defined as

$\psi_s<0$	Accumulation of holes (bands bend upward)
$\psi_s=0$	Flat-band condition
$\psi_B>\psi_s$	Depletion of holes (bands bend downward)
$\psi_s=2\psi_B$	Midgap with $n_s=p_s=n_i$ (intrinsic concentration)
$\psi_s>2\psi_B$	Inversion (electron enhancement, bands bend downward further)

A great deal of information about the MOS system can be obtained from the capacitance- voltage characteristic of the MOS capacitors and the calculation of the total capacitance of the MOS system under different bias conditions will be explained in detail in the following section of this chapter.

3.2 Theoretical Capacitance of Ideal MOS Structure

The analysis of small-signal capacitance of the MOS structure provides valuable insight into the electrical behavior of the oxide-silicon interface and its technology. The measured C-V curve can be compared with an ideal calculated C-V curve that is free of interface states and oxide charges. The differences between these two curves can be used to extract D_{it} and effective oxide charges. The calculation of the ideal C-V curve can be found in many textbooks (Nicollian and Brews, 1982; Schroder, 1998; Cassey,1999)

As compared with parallel plate capacitor, the static and differential capacitances differ for MOS capacitor since the charges change nonlinearly with a small differential change in voltage across the MOS structure. However, like the parallel plate capacitor, the differential changes in charge density occur at the edges of the oxide. For a MOS capacitor the differential capacitance per unit area is given as:

$$C' = \left| \frac{dQ_{Si}}{dV_G} \right| \tag{3.5}$$

since the gate voltage is partially dropped across the oxide and partially across the semiconductor, V_G can be written as:

$$V_G = V_{ox} + \psi_s \tag{3.6}$$

where V_{ox} is the oxide voltage and ψ_s is the surface potential. Similarly oxide voltage can be written as:

$$V_{ox} = \frac{|Q'_{Si}|t_{ox}}{\varepsilon_{ox}} \tag{3.7}$$

The differential capacitance per unit area from Eq. 3.6 and Eq. 3.7 now becomes

$$C'_{dif} = \frac{1}{1/C'_{ox} + 1/\left|\frac{dQ'_{Si}}{d\psi_s}\right|} \tag{3.8}$$

Eq. 3.8 may be written as

$$\frac{1}{C'_{dif}} = \frac{1}{C'_{ox}} + \frac{1}{C'_{Si}} \tag{3.9}$$

where

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad \text{and} \quad C'_{Si} \equiv \left|\frac{dQ'_{Si}}{d\psi_s}\right| \tag{3.10}$$

Eq. 3.9 represents the series combination of a fixed capacitance of the oxide and the variable capacitance of the Si which depends on the applied gate voltage through ψ_s as shown in Figure 3.7.

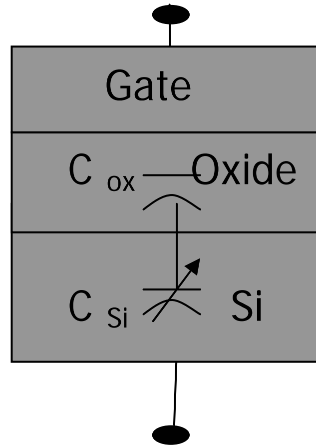


Figure 3.7. Schematic representation of the MOS capacitor as a series combination of C_{ox} and C_{Si}.

The evaluation of C'_{Si} requires representing of Q'_{Si} as a function of ψ_s. In this case potential ψ is defined as zero in the bulk of semiconductor. At the semiconductor surface, $\psi = \psi_s$. The potential ψ as a function of distance can be obtained by using the one-dimensional Poisson equation

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s} \tag{3.11}$$

were ε_s is the permittivity of the semiconductor and $\rho(x)$ is the total space charge density given by

$$\rho(x) = q(N_D^{\ +} - N_A^{\ -} + p_p - n_p) \tag{3.12}$$

where $N_D^{\ +}$ and $N_A^{\ -}$ are the densities of the ionized donors and acceptors respectively. Since in the bulk of the semiconductor, the charge neutrality must exist, $\rho(x)$ and ψ should be equal to zero. Then we have

$$N_D^{\ +} - N_A^{\ -} = n_p - p_p \tag{3.13}$$

for any value of ψ, difference between free carriers

$$p_p - n_p = p_{po}\exp(-\beta\psi) - n_{po}\exp(\beta\psi) \tag{3.14}$$

By replacing Eq. 3.13 and Eq. 3.14 into Eq. 3.12, the relative total space charge density, for $N_A >> N_D$, $p_{po} \approx N_A$, thus $n_{no} \cong n_i^2 / N_A$, can be obtained as

$$\rho(x) = q\left(\frac{n_i^2}{N_A^-} - N_A^- + N_A^- e^{-(\beta\psi)} - \frac{n_i^2}{N_A^-}(e^{(\beta\psi)})\right)$$

the resulting Poisson equation can be obtained as

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\varepsilon_s}[N_A^-(e^{-\beta\psi} - 1) - \frac{n_i^2}{N_A^-}(e^{\beta\psi} - 1)]. \tag{3.15}$$

Integration Eq. 3.15 from the bulk toward the surface obtained as

$$\int_0^{\partial\psi/\partial x}\left(\frac{\partial\psi}{\partial x}\right)d\left(\frac{\partial\psi}{\partial x}\right) = -\left(\frac{qN_A^-}{\varepsilon_s}\right)\int_0^{\psi}\left[(e^{-\beta\psi} - 1) - \left(\frac{n_i^2}{N_A^-}\right)(e^{\beta\psi} - 1)\right]d\psi. \tag{3.16}$$

Eq 3.16 gives the relation between the electric field E_{Si} ($E_{Si} = -\partial\psi/\partial x$) and the surface potential $\psi = \psi_s$:

$$E_{Si}^2 = 2\left(\frac{kT}{q}\right)^2\left(\frac{q^2N_A^-}{\varepsilon_s kT}\right)\left[(e^{-\beta\psi} + \beta\psi - 1) + \left(\frac{n_i}{N_A^-}\right)^2\left(e^{\beta\psi} - \beta\psi - 1\right)\right]. \tag{3.17}$$

here the following abbreviations should be introduced:

$$F\left(\beta\psi, \left(\frac{n_i}{N_A^-}\right)^2\right) \equiv \left[(e^{-\beta\psi} + \beta\psi - 1) + \left(\frac{n_i}{N_A^-}\right)^2(e^{\beta\psi} - \beta\psi - 1)\right]^{1/2}. \tag{3.18}$$

and

$$L_D \equiv \sqrt{\frac{kT\varepsilon_s}{q^2N_A^-}} \tag{3.19}$$

L_D is called the extrinsic Debye length for holes and represent the distance over which the free carriers reduce the potential from the fixed impurity ions. L_D govern the majority carrier deviation from the dopant concentration. Thus the electric field becomes as

$$E_{Si} = \pm \frac{\sqrt{2}kT}{qL_D} F\left(\beta\psi, \left(\frac{n_i}{N_A^{-}} \right)^2 \right) \qquad (3.20)$$

For a static electric field, the space charge per unit area is related to the field through the Gauss law by $Q_{Si} = \varepsilon_s E_{Si}$ which gives

$$Q_{Si} = \pm \frac{\sqrt{2}\varepsilon_s kT}{qL_D} F\left(\beta\psi, \left(\frac{n_i}{N_A^{-}} \right)^2 \right) \qquad (3.21)$$

where a positive sign (+) is applied for the accumulation and a negative sign (-) for the depletion. A typical variation of space charge density in the semiconductor is controlled by F function. Q_{Si} as a function of surface potential ψ_s for a p-type silicon with N_A=1.2x10^{15} cm^{-3} at room temperature is shown in Figure 3.8. For negative ψ_s, Q_{Si} is positive and corresponds to accumulation region. The dominant factor in F function is $\sim \exp(qI\psi_s I / 2kT)$. Flat band condition occurs at $\psi_s = 0$. For $\psi_B > \psi_s > 0$, Q_{Si} is negative and this case corresponds to depletion region and the dominant factor in F function is $\sim \sqrt{\psi_s}$. Inversion case occurs at $\psi_s >> \psi_B$. In this condition Q_{Si} is governed by $\exp(q\psi_s / 2kT)$.

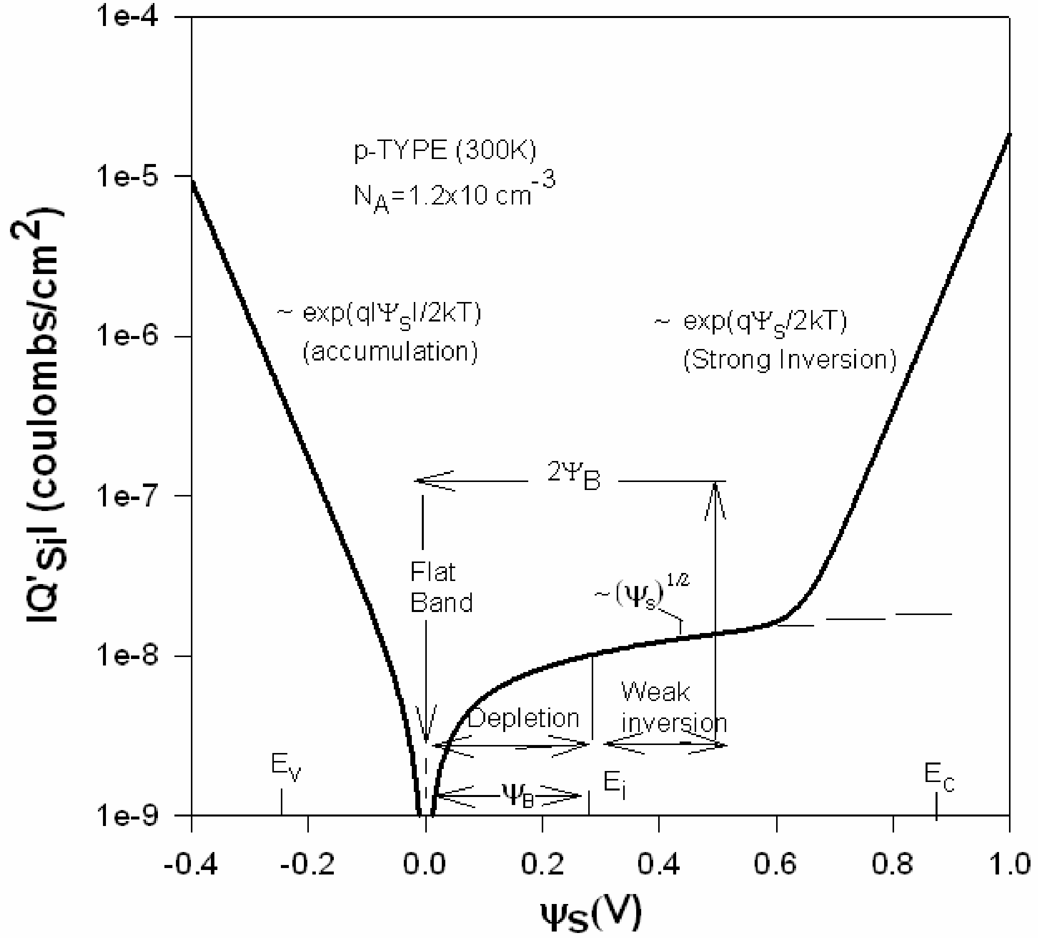


Figure 3.8. Variation of the space charge density Q'_{Si} in the semiconductor as a function of the surface potential ψ_s for a p-type Si with N_A^-=1.2x10^{15} cm^{-3} at room temperature.

The variable capacitance of silicon given in Eq. 3.10 is obtained taking derivative of Eq. 3.21 over ψ_s as

$$C'_{Si} = \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{\left[1 - e^{-\beta\psi_s} + \left(\frac{n_i}{N_A^-}\right)^2 \left(e^{\beta\psi_s} - 1\right)\right]}{F\left(\beta\psi_s, \left(\frac{n_i}{N_A^-}\right)^2\right)} \tag{3.22}$$

At flat-band condition, where ψ_s=0, flat-band capacitance for silicon substrate, C_{FB}' can be obtained by expanding the exponential terms into series as fallows;

$$C_{FB}' = \frac{\varepsilon_s}{L_D} \quad . \tag{3.23}$$

Then the differential capacitance of MOS system given in Eq. 3.9 can be obtained as

$$C_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} L_D} \quad . \tag{3.24}$$

Combination of Eq. 3.6, Eq. 3.9, and Eq. 3.20 gives the complete description of the ideal MOS structure as shown in figure 3.9. For the negative applied gate voltage there is an accumulation of holes and the total differential capacitance is close to oxide capacitance. As the negative gate voltage decreases a depletion region is formed. This region is the region where the total differential capacitance decreases. The capacitance goes through a minimum and then increases again as the inversion layer of electrons form at the surface of the semiconductor. Finally depending on the applied frequency two different behavior of MOS structure can be observed. At very small frequencies between 5 to 100 Hz, the electron concentration at the surface of the surface of semiconductor has the ability to follow the applied ac voltage and this lead to charge exchange with the inversion layer. Thus the total differential capacitance increases and reaches back its maximum value as seen in Figure 3.9a. However for frequency higher than 100 Hz since the electron could not follow the signal no increase in total differential capacitance can be observed as shown in Figure 3.9b.

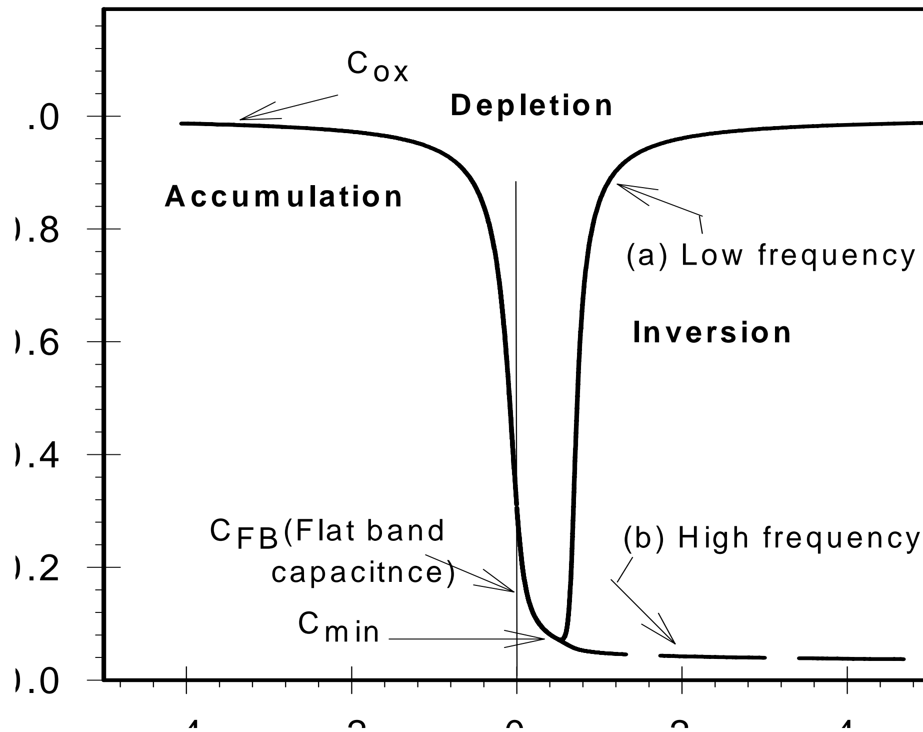


Figure 3.9. Normalized Theoretical ideal MOS structure C-V curve for accumulation, depletion and inversion region

3.3 Non-Ideal MOS Capacitor

In the above discussion concerning C-V characteristics we have assumed that there is zero charge trapped in the oxide and also there is no charge trapped at the oxide-semiconductor interface which are known as non ideal effect. In this section the non ideal effect and its analysis will be discussed.

3.3.1 Non-Ideal Effect

In an actual MOS capacitor there are several non-ideal effects which affect the conduction mechanism of the capacitor. These non-ideal effects are oxide charges, interface trap charges and the work function difference between metal and semiconductor. Figure 3.10 shows the common terminology for oxide and interface charge. Oxide charges can be collected in three groups as fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and mobile ionic charge (Q_m).

Fixed oxide charge Q'_f, is due to structural defect in the oxide layer less than $25A^o$ from the oxide/Si interface. This is a positive charge and its density is related to the oxidation process.

Oxide trap charge Q'_{ot}, can be obtained as positive or negative due to holes or electrons trapped in the bulk of the insulator. This trapped charge may result from ionizing radiation or avalanche injection.

The mobile ionic charge, Q'_m, is obtained because of the ionic impurities such as Li^+, Na^+, and K^+.

These charges may alter the threshold voltage, silicon surface potential and thereby change reverse leakage current and finally affects the avalanche breakdown voltage. The sum of these oxide charges is called effective oxide charge Q_{eff} (and its number density N_{eff}) as given in Equation 3.25.

$$Q_{eff} = Q_f + Q_m + Q_{ot} \tag{3.25}$$

Interface trapped charges Q_{it} and more importantly interface trap charge density, D_{it}, plays the major role in the operation of MOS devices. These charges cause the recombination of free carriers in the conduction and valence bands. These charges present in the structure due to structural and oxidation-induced defects such as, metal impurities, radiation or bond-breaking process. And they have been shown to exist within the forbidden gap due to interruption of the periodic lattice structures of the surface of a crystal. The interface trap charge can be obtained as positive or negative and they are in electrical communication with the underlying Si. This charge can also be called as surface states, fast states or interface states.

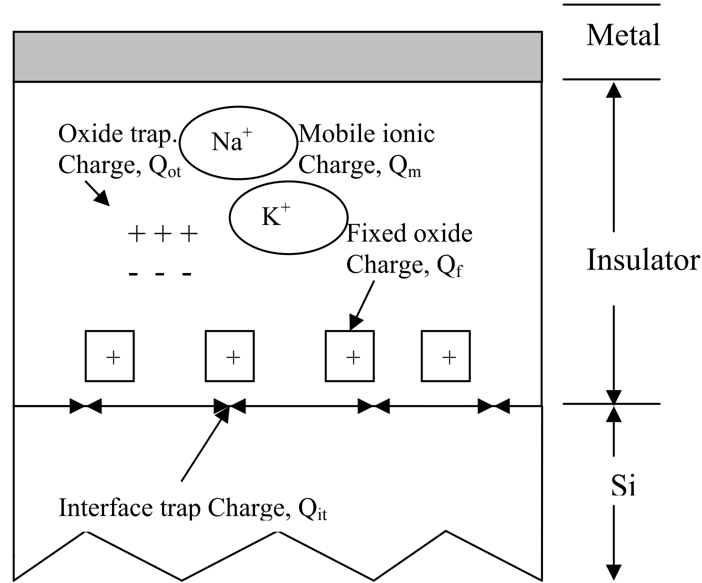


Figure 3.10. Schematic illustration of non-ideal effects present in Metal-Oxide-Si system.

On the other hand, the work function differences exist due to changes in doping concentration of p-type substrate which modifies the position of Fermi level in semiconductor. The workfunction differences can be overcome by applying external gate voltage which produce flat band and is represented as V^{o}_{FB}. And as it was mentioned at section 3.1, flat band voltage is the work function differences of MOS structure without oxide or interface trapped charges which is given as

$$V^{o}_{FB} = \Phi_{ms} = \Phi_{m} - \Phi_{s} = \Phi_{m} - (\chi + \frac{E}{2q} \pm \psi_{B}) \tag{3.26}$$

However, because of the doping level of the semiconductor and other non ideal effect, here V^{o}_{FB} is not zero, instead it can be positive or negative number which gives the polarity connected to the metal to obtain the flat band condition.

The non ideal effects, mentioned above changes all the characteristics of the MOS capacitor. A great deal of information about these non-ideal effects present in MOS capacitors can be obtained from the capacitance-voltage characteristics of MOS device. The density of effective oxide charge is obtained from the flat band V_{FB} voltage shift and the density of interface trap charges is calculated from the Therman's method

"(Nicollian and Brews, 1982)". In order to determine the quality of the gate oxide, these curves with Therman's method are used extensively as a diagnostic tool.

3.3.2 Calculation of Flat Band Voltage, Doping concentration and the Effective Oxide Charge

In the previous section, effective oxide charges were described in detail. These charges affect the experimental C-V curve of MOS capacitor. They cause a shift of the ideal MOS curve along the voltage axis. Consequently a larger voltage is required to set up the surface potential ψ_s on semiconductor surface. The new flat band voltage with these oxide charges can be obtained as

$$V_{FB} = \Phi_{ms} + \frac{Q_{eff}}{C'_{ox}} = V_{FB}{}^{o} + \frac{Q_{eff}}{C'_{ox}} \tag{3.27}$$

where Φ_{ms} is work function differences as defined in Eq. 3.26. Q_{eff} is effective oxide charge as defined in Eq. 3.25and C_{ox} is the oxide capacitance.

One of the methods to obtain flat band voltage is to plot experimentally obtained $(1/C^2)$ versus V_G curve. This curve provides with flat band voltage and doping concentration N_A of p-type substrate. An example of $(1/C^2)$ versus V_G is shown in Figure 3.11. The intercept point in the voltage axis is the flat band voltage $V_{FB,}$ and the slope of the curve gives the doping concentration.

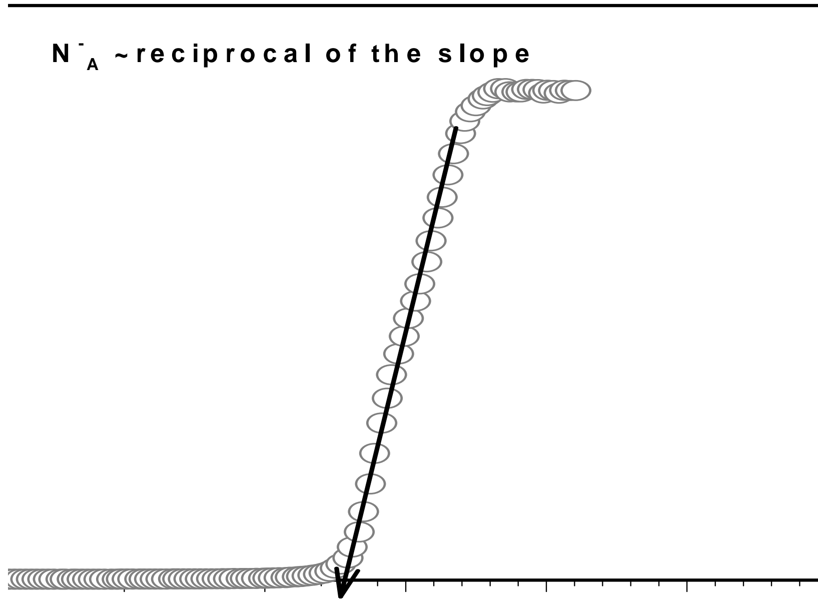


Figure 3.11. $1/C^2$ versus V_G curve of a MOS capacitor

In accumulation and inversion, free carrier charge density is only weakly dependent on doping concentration. Therefore doping concentration cannot be obtained accurately in either accumulation or inversion. Therefore it can be obtained accurately in depletion, where free carrier concentration strongly depends on doping concentration. The slope in Figure 3.11 is taken for depletion region. Doping concentration is calculated using the following equation

$$N^-{}_A = -2\left[q\varepsilon_s \frac{d}{dV_G}\left(\frac{1}{C^2}\right)\right]^{-1} \tag{3.28}$$

Eq. 3.28 shows that N_A^- is related reciprocally to the slope of a $(1/C^2)$ versus V_G curve. A positive slope will give a negative N_A^- from Eq. 3.28 for acceptors whereas a negative slope gives a positive N_A^- for donors.

Another common method of measuring the flat band voltage V_{FB} is comparing experimental and theoretical (ideal) C-V curves. The theoretical C-V curve is calculated for a device without work function difference or oxide charges together with

the oxide thickness, dielectric constant and doping concentration N_A obtained from the experimental C-V curve of the same MOS device. Then both C-V curves are plotted together on the same figure. The shift of experimental capacitance from that at $V_G=0$ Volt is indicated as the flat band voltage shift V_{FB} as shown in Figure 3.12. For each MOS device, the V_{FB} values are obtained by using the $1/C^2$ vs V_G curve and from the comparison of both ideal and experimental C-V curves. Consistent values of VFB are obtained from both method within the experimental and human error.

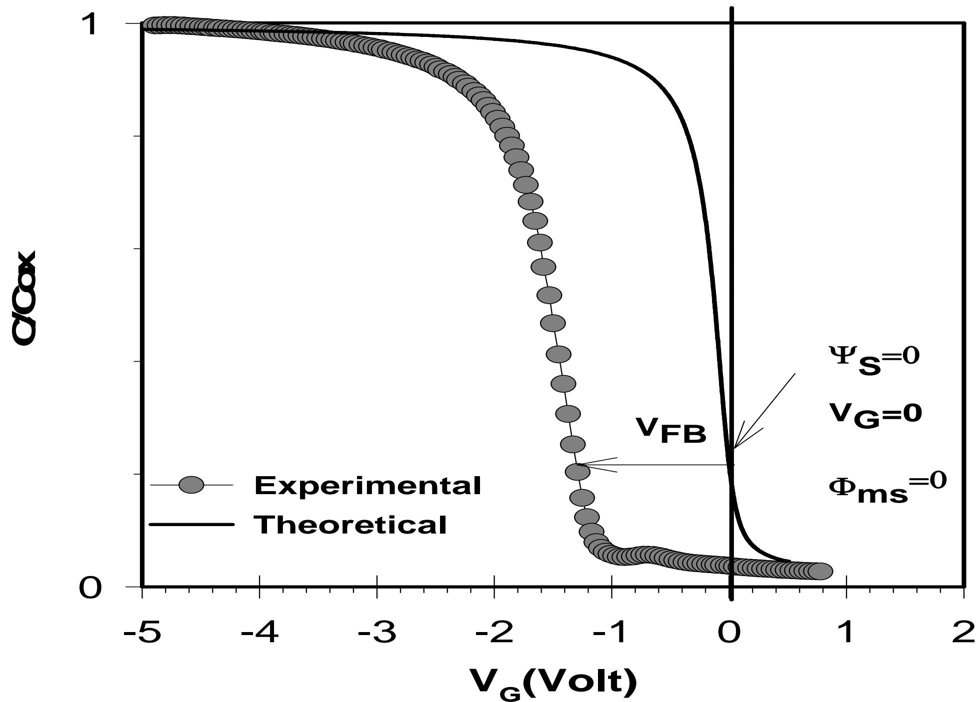


Figure 3.12. Theoretical and experimental high Frequency C-V curves of a MOS capacitor with p-type silicon substrate.

Once the flat band voltage is obtained from the shift of theoretical and experimental C-V curves, effective oxide charge Q_{eff} and its number density N_{eff} are calculated using the equation given below:

$$N_{eff} = \frac{Q_{eff}}{q} = \frac{C'_{ox}(V^{o}_{FB} - V_{FB})}{q} \tag{3.29}$$

In addition, some of the charges presented in the oxide are mobile trap charges and follows the sign of applied gate voltage. They move toward metal gate or to

semiconductor or the polarity of gate voltage changes. The effect of moving charges is measured by using double sweep measurement of high frequency C-V curve. In this method, capacitance is measured from accumulation to inversion and then from inversion to accumulation by changing the polarity of gate voltage V_G. A hysteresis type C-V curve is obtained if mobile trap present in the oxide as shown in Figure 3.13. Depending on the sign of mobile trap charges, clockwise or counterclockwise hysteresis is measured. An example of counter-clockwise hysteresis is shown in Figure 3.13. The nature of counterclockwise hysteresis attributed to the existing of the positive mobile trap charges and clockwise hysteresis indicates the existing of negative mobile trap charges present in the oxide. The density of the positive mobile trap charges can be found with the help of ΔV_{FB}, the voltage shift between forward and reverse bias C-V measurement shown in Figure 3.13, oxide capacitance C_{ox}, electron charge, q and gate area A as given below;

$$N_{mobile} = \frac{C_{ox} \Delta V_{FB}}{qA} \tag{3.30}$$

As an example shown in Figure 3.13, the density of mobile trap charges, N_{mobile}, calculated from 600 mV flat band voltage shift, is found to be 1.13×10^{12} cm^{-2} by using the values of C_{ox}=189 pF, $A=6.25 \times 10^{-4} cm^2$ and $q=1.6 \times 10^{-19}$ C.

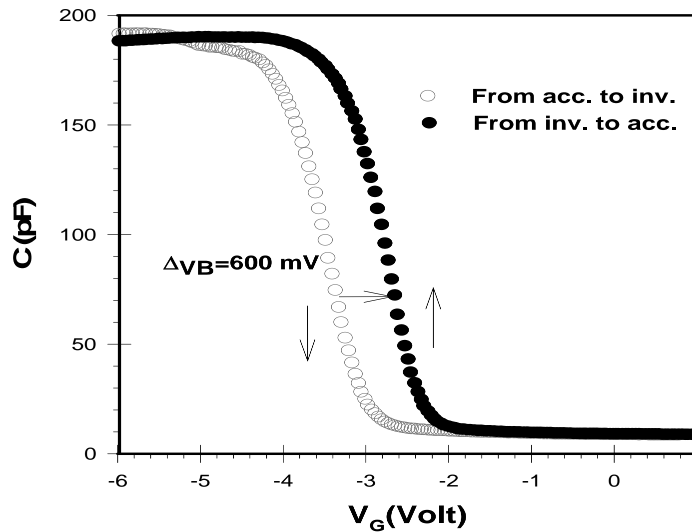


Figure.3.13. Hysteresis behavior of high frequency C-V curve of MOS capacitor

3.3.3 Extraction of Density of Interface Trap States (D_{it})

Interface defect states, or interface traps, are the defects located at the interface between the Si substrate and the gate dielectric layer. Interface trap density, D_{it}, depends on the gate dielectric material as well as the fabrication technique. D_{it} is a crucial parameter for the effectiveness of the fabrication process as well as the device performance. In this section methods used to derive the D_{it} levels of MOS capacitor are explained in detail. These are high frequency C-V method known as Terman's method and simultaneous C-V method.

3.3.3.1 High Frequency Capacitance-Voltage Method (Terman's Method)

High frequency C-V method was first used by Terman to calculate D_{it} levels. In this method, both high frequency experimental and theoretical (ideal) capacitance-voltage curves are used to calculate D_{it} levels. Here both experimental and theoretical C-V curves are normalized to the oxide capacitance C_{ox} to compare the effects of interface trap states. In Figure 3.14 an example of both experimental C/C_{ox} versus V_G and theoretical C/C_{ox} versus surface potential ψ_s are shown together. In ideal C/C_{ox} curve, there is no effect due to interface traps charges, however, experimental C/C_{ox} curve shifts along voltage axis due to interface trap present in actual MOS devices. By comparing these curves, the effect of interface traps on C-V curve is obtained by obtaining the functional dependence of surface potential ψ_s on gate voltage V_G for every C/C_{ox} normalized capacitance values shown in Figure 3.14. Theoretical C versus ψ_s values are calculated by using the Eq. 3.13 through 3.22 given in this chapter.

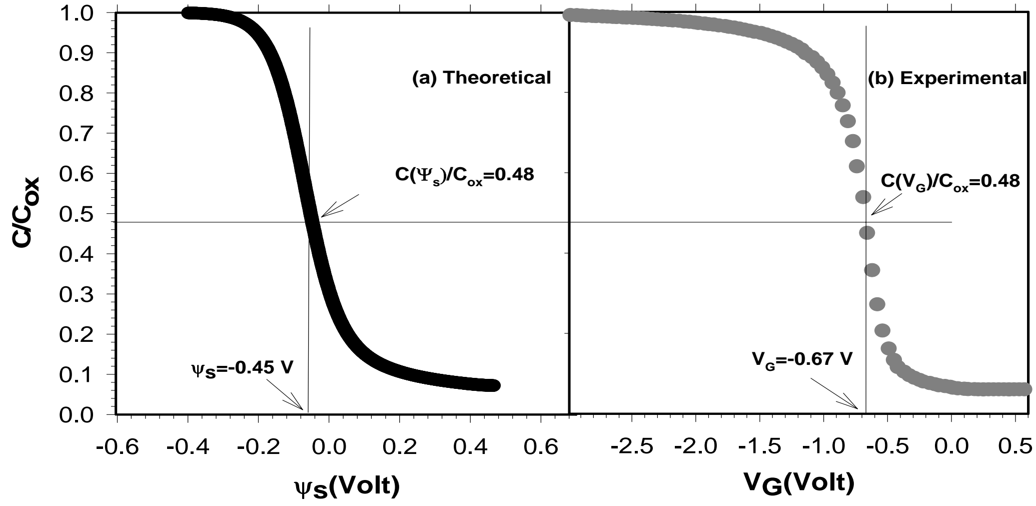


Figure 3.14. (a) Theoretical C/C_{ox} vs surface potential ψ_s, and (b) experimental high frequency C/C_{ox} vs gate voltage V_G for a MOS capacitor.

The resulting ψ_s versus V_G curve obtained from the data shown in Figure 3.14 is shown in Figure 3.15. This curve contains all necessary information about the interface trap states present at the interface of gate oxide and silicon substrate. As shown in Figure, functional dependence of ψ_s on V_G is not linear, the slope changes point by point. By using the oxide capacitance C_{ox} the slope $\frac{d\psi_s}{dV_G}$ and capacitance of silicon depletion layer $C_{Si}(\psi_s)$, interface trap capacitance C_{it} is calculated as

$$C_{it} = C_{ox}\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1} - 1\right] - C_{Si}(\psi_s)$$

(3.31)

Finally, the density of interface trap states, D_{it}, is found as:

$$D_{it} = \frac{C_{it}(\psi_s)}{q} = \frac{C_{ox}}{q}\left(\frac{dV_G}{d\psi_s} - 1\right) - \frac{C_{Si}}{q}$$

(3.32)

After calculation of D_{it} values for every ψ_s, corresponding energy level E in the band gap of crystalline silicon is found for each ψ_s value. In order to present the energy position of D_{it} levels in the band gap of crystalline silicon, D_{it} (#/cm^{2}eV) versus E

energy (eV) is plotted as shown in Figure 3.16 as a final quality criteria of oxide-silicon interface in a MOS device. Finally MOS devices with different oxide layers and prepared with different surface treatment methods are compared using the D_{it} versus energy results calculated from the Therman's method.

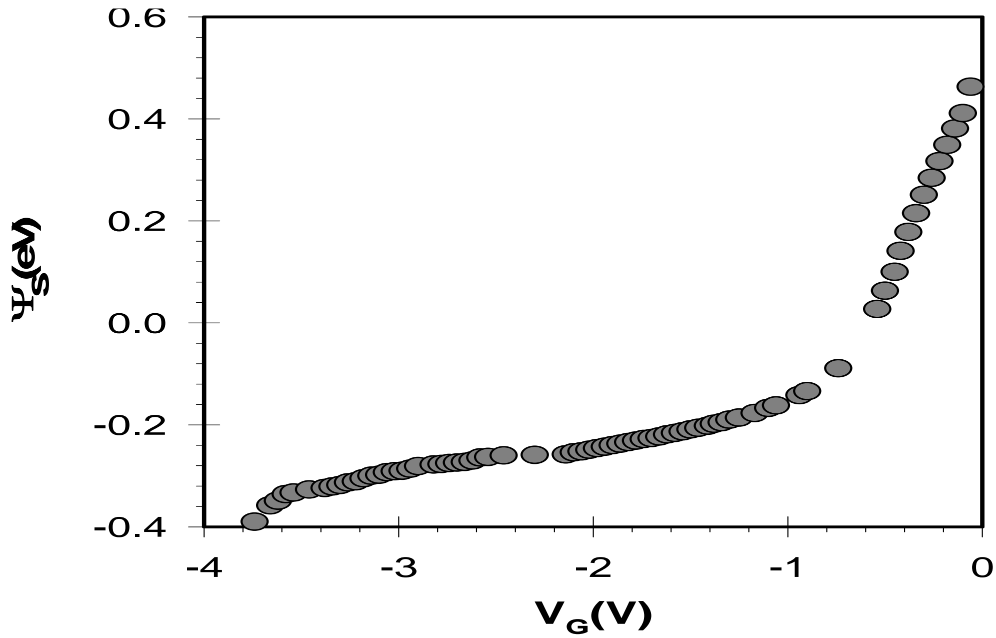


Figure 3.15. The surface potential ψ_s versus gate voltage V_G obtained from the theoretical and experimental high frequency C/C_{ox} curves of a MOS capacitor shown in Figure 3.14

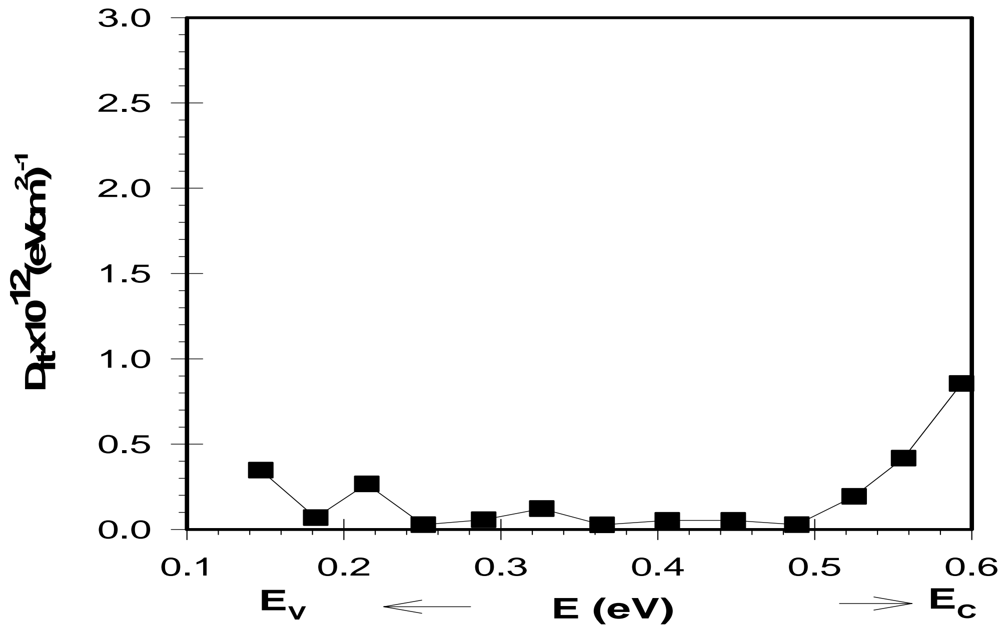


Figure 3.16. Density of interface trap states, D_{it}, as a function of energy in the band gap of crystalline silicon obtained from Figure 3.1

3.3.3.2 Combined High-Low Frequency Capacitance Method-Simultaneous Capacitance –Voltage Spectroscopy

The calculation of the ideal C-V curve is not only time consuming, but also introduces uncertainty for very thin gate dielectrics. Combination of a high frequency C-V curve with a low frequency C-V curve which avoids the ideal C-V calculation was first achieved by Costagne and Vapile (Nicollian and Brews, 1982). Theoretical computation of C_{Si} and measurement of doping profile is eliminated in this method. From high frequency C-V, high frequency capacitance C_{HF} is obtained as;

$$C_{HF} = \frac{C_{ox}C_{Si}}{C_{ox} + C_{Si}} \tag{3.33}$$

Then, C_{Si} is derived as;

$$C_{Si} = \frac{C_{ox}C_{HF}}{C_{ox} - C_{HF}} \tag{3.34}$$

At low frequencies, interface trap capacitance C_{it} can be extracted from the measured low frequency capacitance if C_{Si} and C_{ox} are known. The relation between these capacitances can be written as

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{Si} + C_{it}} \tag{3.35}$$

where C_{LF} is the low frequency capacitance measured at gate bias V_G. Solving Eq. 3.34 for C_{it} yields

$$C_{it} = \left[\frac{1}{C_{lf}} - \frac{1}{C_{ox}}\right]^{-1} - C_{Si} \tag{3.36}$$

where C_{ox} can be measured in strong accumulation. Combining Eq. 3.34 and Eq 3.36 yields

$$C_{it} = \left[\frac{1}{C_{lf}} - \frac{1}{C_{ox}} \right]^{-1} - \frac{C_{ox} C_{HF}}{C_{ox} - C_{HF}} \qquad (3.37)$$

In this way C_{it} is obtained directly from the measured C-V curves, without the uncertainty introduced by a theoretical C_{Si} and without uncertainty as to whether C_{Si} has been calculated for the correct band bending. The density of interface states, D_{it}, is calculated with the help of Eq. 3.32 where $D_{it}= C_{it}/q$ together with Eq.3.37.Examples of C_{HF} and C_{LF} versus V_G and D_{it} versus E obtained from both Terman's method and simultaneous C-V method are shown in Figure 3.17 and Figure3.18, respectively.

For samples with SiO_2, the density of interface trap states obtained from both Terman's method and Simultaneous C-V method are agree very well as shown in Figure 3.18 and the experimental error is within the limit of %10. However, as discussed before, a low frequency C-V curve is not always available for an ultra thin high k gate dielectric layer with a large leakage current. In addition, the leakage current, which either adds to or subtracts from the displacement current, usually distorts the resulting C-V curve. Therefore accumulation capacitance is not exactly the same as the inversion capacitance (Schroder, 1998). Due to these reasons, Simultaneous C-V method could not be carried out for high-k gate oxide.

In this thesis, the density of interface trap states of Al-SiO_2-Si MOS capacitors are evaluated by using both Terman's method and combined high and low frequency method. However, for the determination of interface trap states of Metal-Ta_2O_5-Si MOS capacitors only Terman's method is used. The details about the results will be given in the next chapter.

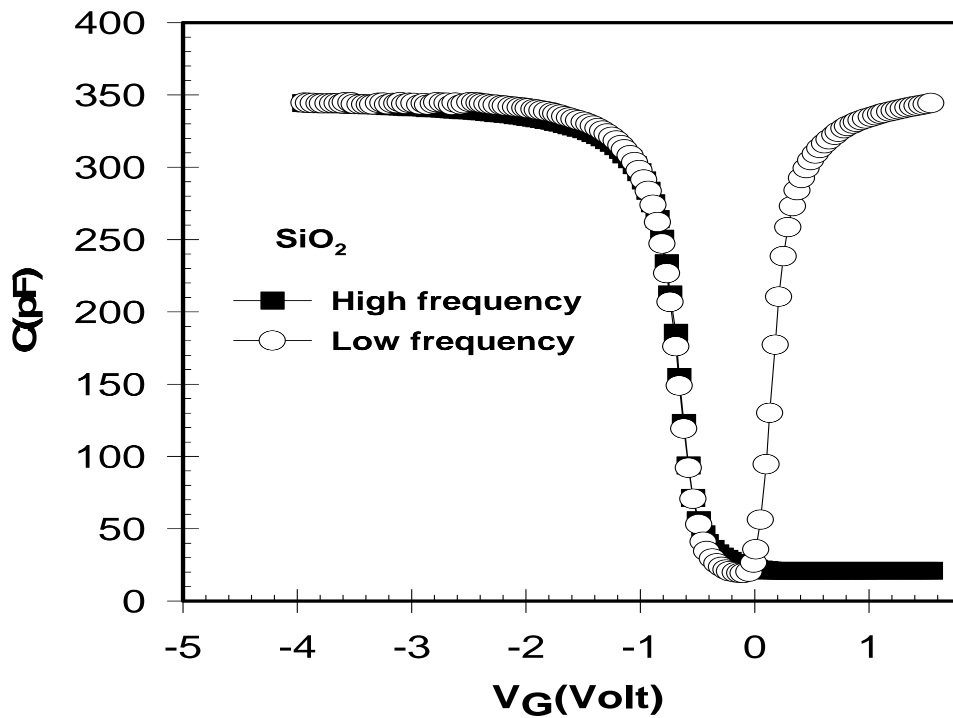
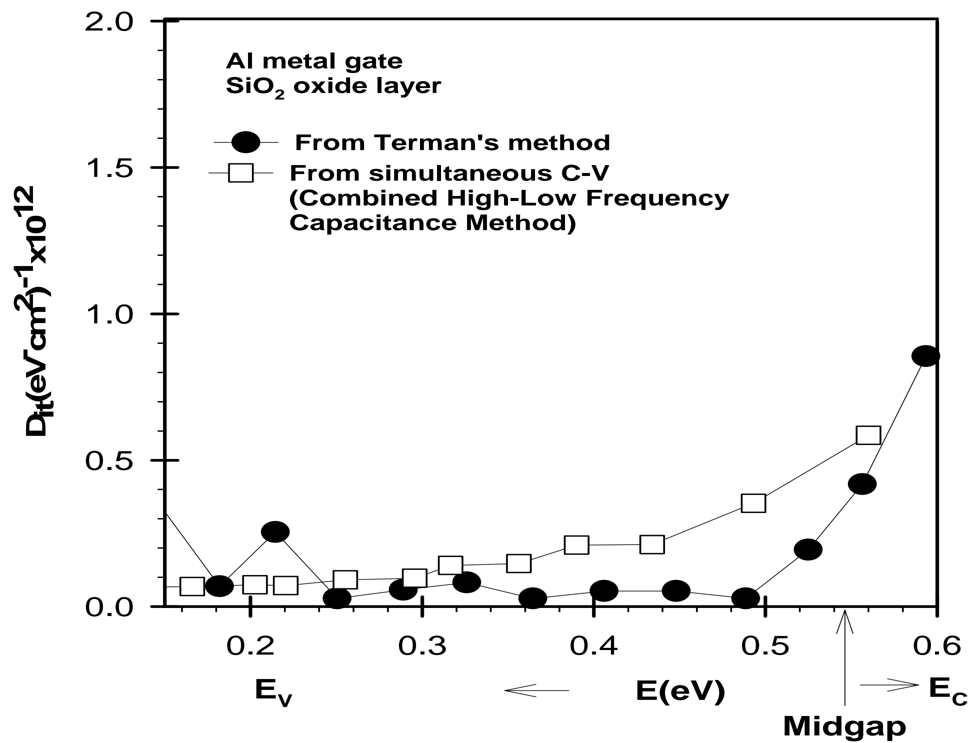


Figure 3.17. Combined High-low frequency C-V curves for native SiO_2 sample



igure 3.18 Density of interface trap states, D_{it}, as a function of energy in the band gap of crystalline silicon obtained from Terman's method and Combined High-low frequency Capacitance method for sample with SiO_2 oxide layer

CHAPTER 4

EXPERIMENTAL RESULTS

4.1 Introduction

Ta_2O_5 has been one of the most promising high–k dielectric materials to replace SiO_2 in sub micron IC devices due to its high dielectric constant and chemical stability during the processing. Electrical properties of Ta_2O_5 oxide layers grown on top of silicon surface and that of Ta_2O_5-silicon interface are controlled by the processing techniques. Detailed understanding of high-k oxide on silicon surface, the effect of different metal gates on the oxide and interface properties of oxide-silicon structure requires additional investigation. In this thesis, a prior nitridation process of silicon surface using rapid thermal nitridation method in N_2O and NH_3 gas before formation of Ta_2O_5 oxide is used. In addition, different metal gates such as Al, TiN and W were used to investigate the effects of metal gate-oxide interface on C-V characteristics.

The first and second part of this chapter is devoted to electrical characterization of the samples with native SiO_2 and Ta_2O_5 oxide formed on unnitrided silicon substrate with Al top metal gate. These samples are represented as reference sample-1 and reference sample-2. The third part of the chapter is devoted to effect of prior nitridation of silicon surface before formation of Ta_2O_5 oxide layer. In this part, two different nitridation processes in N_2O and NH_3 using RTN at different nitridation temperatures will be introduced and details of the measured parameters will be given. In the last part, the effect of gate metal on the characteristics of MOS capacitors prepared with the nitrided and unnitrided silicon surface will be investigated. The electrical characterization is carried out using high frequency C-V spectroscopy. In addition, conductances versus gate voltage and leakage current density measurements are also carried out simultaneously at the same frequency. Important device parameters regarding doping concentration, flat band voltage, dielectric constant, hysteresis behavior, equivalent oxide thickness, effective oxide charge were derived for every sample. The interface trap state density which is important for characterizing a high-k dielectric material in MOS devices is derived from the Terman's method "(Nicollian and Brews, 1982)". Finally, the results are compared with the results of the Al-SiO_2-Si

and Al-Ta_2O_5-Si MOS capacitors as reference sample-1 and reference sample-2, respectively.

4.2 Results of Al-SiO_2-Si MOS capacitor; Reference Sample-1

The experimental high frequency and low frequency C-V measurement of four different dots of Al-SiO_2-Si MOS capacitor for the same substrate are shown in Figure 4.1. In the accumulation, both low and high frequency C-V curves overlap, giving the value of oxide capacitance until depletion region. Both curves overlap at negative voltages but they show expected deviation in inversion region, where high frequency C-V curve shows saturation at minimum capacitance value. However, low frequency C-V curve increases until it reaches to accumulation capacitance value. The oxide capacitance, C_{ox}, was obtained around 350 pF. The relative dielectric constant was calculated from the C_{ox} and measured thickness and capacitor area. It is found to be 3.95 as expected for the native oxide SiO_2.

Experimental high frequency C-V curve contains both ideal and non-ideal effects. One of these non-ideal effects in MOS capacitors is the mobile trapped charges. The effect of mobile trapped charges is seen in the hysteresis effect on C-V curve. For this reason, high frequency C-V curve is measured from accumulation to inversion and reversed back to accumulation. After this measurement cycle, depending on the nature of mobile trapped charges present in the oxide, C-V curve shows a shift along clockwise or counterclockwise. The hysteresis effect of dot-2 of Al-SiO_2-Si capacitors is shown in Figure 4.2. It is seen that C-V curves for both measurement cycles overlap quite well, giving ΔV_{FB} shift less than 30 mV. This indicates that native oxide SiO_2 is close to electronic quality, for which ΔV_{FB} is around 20 mV as reported in literature (T. P. Ma, 1997).

Other non ideal effects contributing to high frequency C-V curve of MOS capacitors are work function differences, effective oxide charges and interface trap states. In order to determine the oxide and oxide-silicon interface quality, theoretical (ideal) capacitance-voltage curve of the MOS capacitor is calculated using the

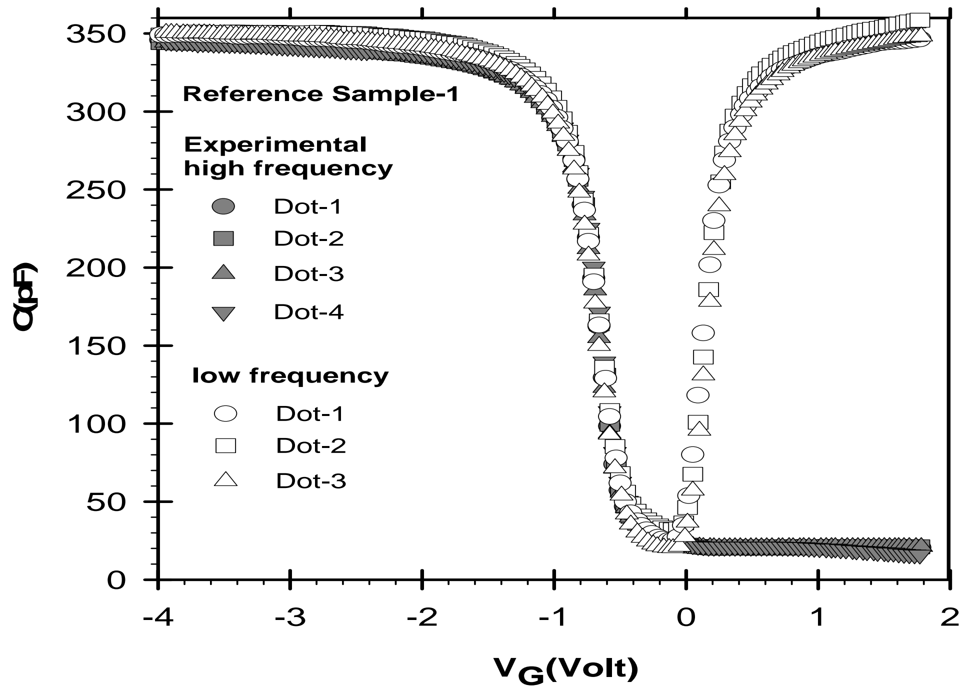


Figure 4.1. Experimental High-Low frequency capacitance versus gate voltage curves of Al- SiO_2-Si MOS capacitors; reference sample

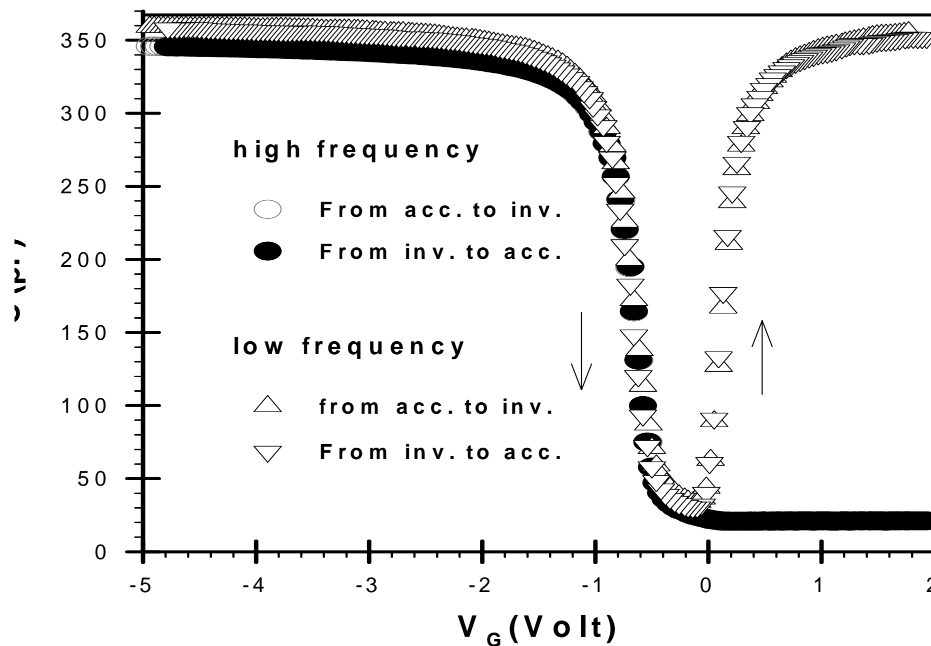


Figure 4.2. Forward and reverse C-V curve of Al- SiO_2-Si MOS capacitor with unnitrided Si surface

experimental value of doping concentration N_A of silicon substrate, oxide thickness and metal gate area. Doping concentration is obtained from the slope of $1/C^2$ versus gate voltage as presented in Figure 4.3. For four different dots, according to equation 3.28, given in Chapter 3, the slope of curves gives the value of N_A to be $9x10^{14}$ cm^{-3}. The intercept of the slope on the V_G axis indicates the shift of flat band voltage V_{FB} due to non-ideal effects.

Ideal and experimental high frequency C-V curves (normalized to oxide capacitance C_{ox}) of one of the MOS capacitor are presented in Figure 4.4. It is seen that experimental C-V curve (symbols) shift to negative voltages due to effective oxide charges present in the oxide layer. The amount of shift, V_{FB}, is measured from V_G=0 volt at ideal curve to experimental C-V curve. The V_{FB} value obtained from Figure 4.4 is around 0.6 volt, which is almost identical to that found from the intercept of slope $1/C^2$ vs V_G shown in Figure 4.3. In addition, further confirmation of V_{FB} voltage is found from the Conductance versus V_G curve simultaneously measured at 1 MHz frequency. In Figure 4.4, conductance G versus gate voltage V_G of the sample is presented on the same figure that it shows a maximum value around the flat band voltage, $V_{FB,}$ as expected for the MOS capacitor. As seen from the figure, capacitance varies from an upper to lower value over the illustrated bias range, whereas equivalent conductance goes through a peak and approach zero on other side. Similar results were also obtained for other dots measured from the same substrate. It can be concluded that experimental C-V and G-V measurements are consistent for a good quality MOS capacitor. On the other hand, from the figure it can be seen that the conductivity of the SiO_2 insulating layer is around 20 μS which is sufficiently low for a good insulating properties. Flat band voltage shift V_{FB} obtained from the shift of experimental curve are used to calculate the effective oxide charge and its number density N_{eff}, present in the native oxide SiO_2 for all the samples using equation 3.29. Calculated N_{eff} values are $2.9x10^{11}$ cm^{-2} for all the samples. These values indicate that SiO_2 has lower effective oxide charge closer to the electronic grade SiO_2 levels reported in literature (Manchanda et all, 1998).

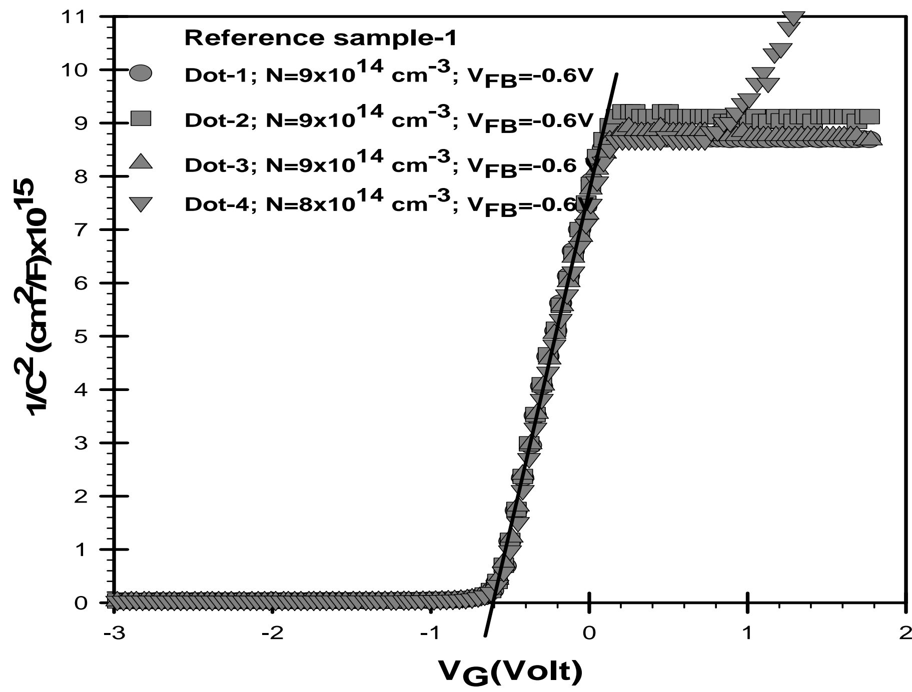


Figure 4.3. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of Al-SiO_2-Si MOS capacitor

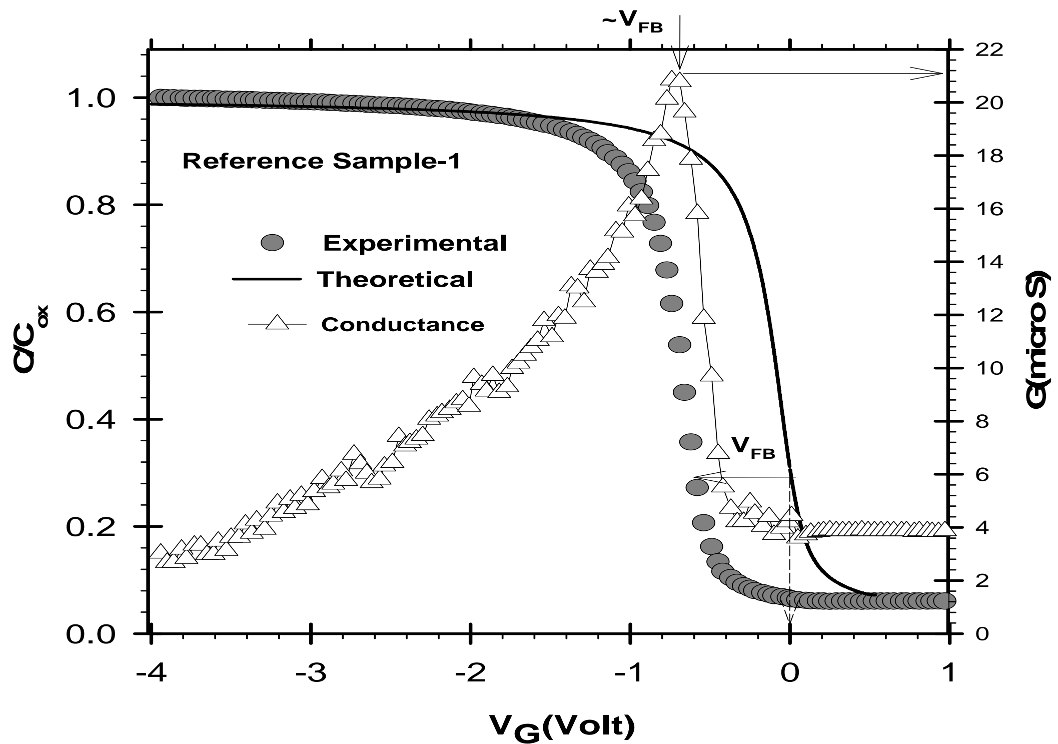


Figure 4.4. Normalized experimental and theoretical capacitance versus gate voltage and conductance versus gate voltage of Al-SiO_2-Si MOS capacitor

Furthermore, the most important non-ideal effect seen in MOS capacitors is the density of interface trap states, D_{it}. The levels of Dit in different dots are calculated using both Terman's method (L. M. Terman, 1962) and simultaneous C-V method. In Therman's method, ideal C/C_{ox} versus surface potential ψ_s and experimental C/C_{ox} versus gate voltage V_G curves are plotted together. From these curves surface potential ψ_s versus gate voltage V_G curve is generated for each sample as shown in Figure 4.5. D_{it} levels of the samples are then calculated using the data in Figure 4.5 and procedure given in Chapter 3. Calculated levels of D_{it} for four different dots and one calculated from simultaneous C-V method are presented in Figure 4.6 as a function of energy in the band gap of silicon. D_{it} levels obtained from both method agree very well and vary around $2 \pm 1 x 10^{11}$ $(eVcm^2)^{-1}$ for all the samples. These values are presented in Table 4.1. These values are low and closer to the value reported for electronic grade of SiO_2-Si interface (P. K. Roy and I. C. Kizilyali, 1998).

Finally, the main characteristics of a MOS capacitors used in IC technology is the leakage current levels measurement through the oxide. Current density J versus gate voltage curve derived from the conductance versus gate voltage curve of the same sample is presented in Figure 4.7. The current density at V_G=0 volt reaches to 60 μAcm^{-2} for sample Dot-1. Other samples also show similar leakage current levels.

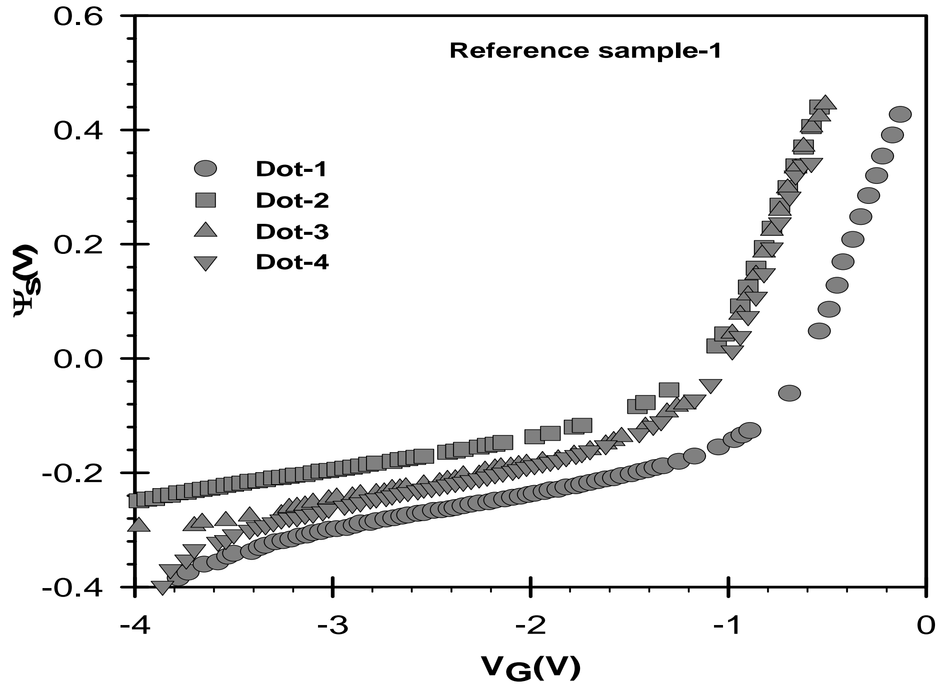


Figure 4.5. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox}-V curves of Al- SiO_2-Si MOS capacitor

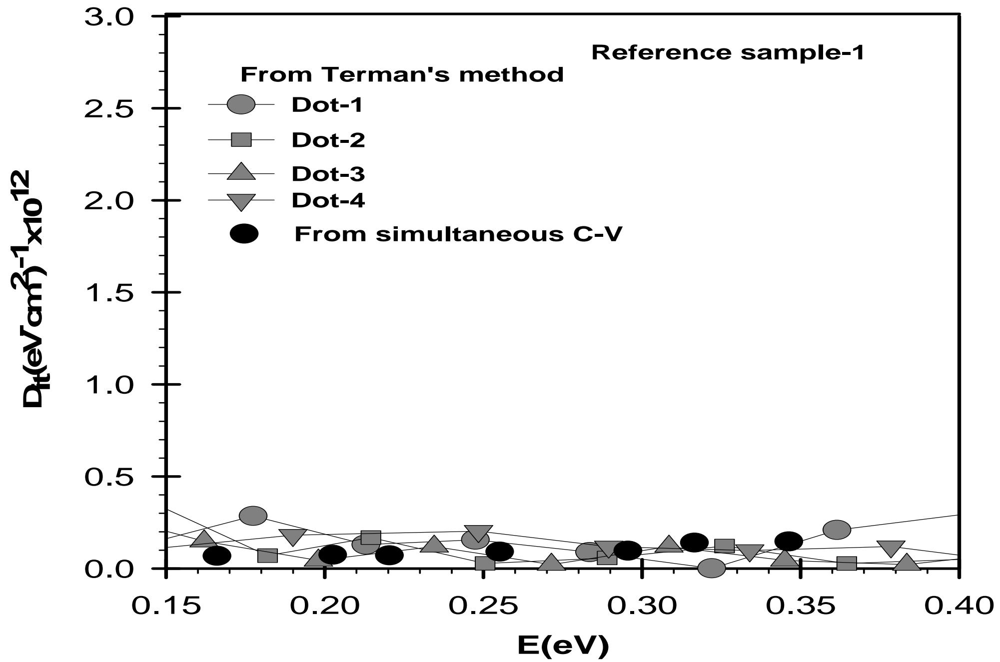


Figure 4.6. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al- SiO_2-Si MOS capacitor

Table 4.1. Summary of parameter extracted from experimental high frequency C-V measurements of Al-SiO_2-Si MOS capacitor; reference sample-1

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} $(eVcm^2)^{-1}$
Dot-1	20	1.96 x10^{-3}	3.9	347	-0.9	-0.6	-0.6	2.9	2 ± 1
Dot-2			3.9	345	-0.9	-0.6	-0.6	2.9	2 ± 1
Dot-3			3.9	344	-0.9	-0.6	-0.6	2.9	2
Dot-4			3.9	344	-0.8	-0.6	-0.6	2.9	2

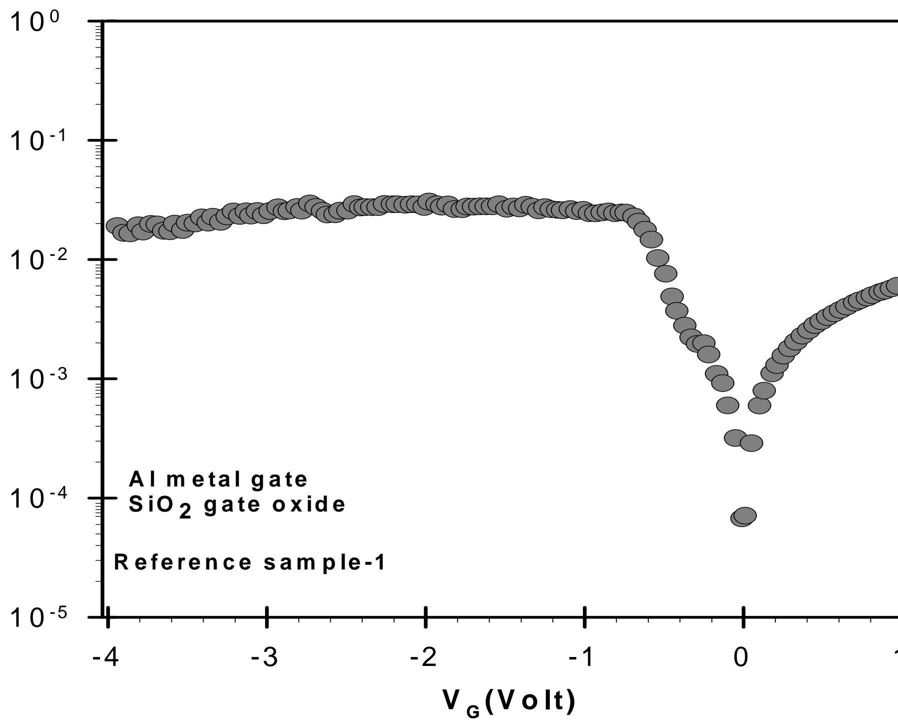


Figure 4.7. J-V characteristics of Al- SiO_2-Si MOS capacitor; reference sample-1.

4.3 Results of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor; Reference Sample-2

It was presented in previous section that reference sample-1 with native oxide has good electronic quality with low effective oxide charge and good quality Si-SiO_2 interface. The replacement of native oxide SiO_2 with high-k dielectrics is important as the thickness of gate oxide decrease below sub-micron levels. The second reference sample is prepared using Ta_2O_5 gate oxide on silicon without any surface treatment of silicon surface before oxidation process. In oxidation process, as described in chapter 2, Ta thin film on silicon is first prepared with RF sputtering process and then oxidized thermally to form Ta_2O_5 oxide in dry oxidation process. Reference sample-2 with Al metal gate has been characterized in detail using several dots from the same substrate.

1 MHz high frequency C-V measurements of four different dots for reference sample 2 are presented in Figure 4.8. The oxide capacitance C_{ox} corresponding to accumulation region almost equals to 310±10 pF for different dots. However, the quasi-static capacitance measurement of this sample could not be achieved due to high level of leakage current. The dielectric constant obtained from the high frequency oxide capacitance value is 11.5 which is higher than that of native oxide SiO_2. The equivalent oxide thickness of a SiO_2 layer that would give the same value of C_{ox} can be obtained from the equation, $t_{eq}=\varepsilon_o \varepsilon_s A/C_{ox}$ (Novkovski et al. 2005), where A is the gate area, ε_o and ε_s is the relative permittivity and dielectric constant of SiO_2. For reference sample-2, calculated equivalent oxide thickness t_{eq} is 6.8±0.3 nm. Further, it is determined from the small variations in accumulation capacitance that the electrical thickness of the gate oxide varied by less than 4 ^{o}A. This indicates that no severe inter-reaction between the gate electrode and gate oxide has occurred.

The first non-ideal effect on C-V curve of reference sample-2 is shown in Figure 4.9, in which hysteresis effect of high frequency C-V measurement is presented. It shows a negligible counterclockwise hysteresis with a 20 mV of ΔV_{FB} voltage shift. This indicates that mobile trap charges in oxide are low and the quality of thermal Ta_2O_5 oxide layer is close to that of native SiO_2 used in reference sample-1.

In order to understand the effect of other non-ideal effects, doping concentration of silicon substrate has been calculated from the slope of $1/C^2$ versus V_G gate voltage. In Figure 4.10 $1/C^2$ vs V_G results of four different dots from the same substrate of reference sample-2 with Ta_2O_5 thermal oxide are presented. Acceptor concentration N_A

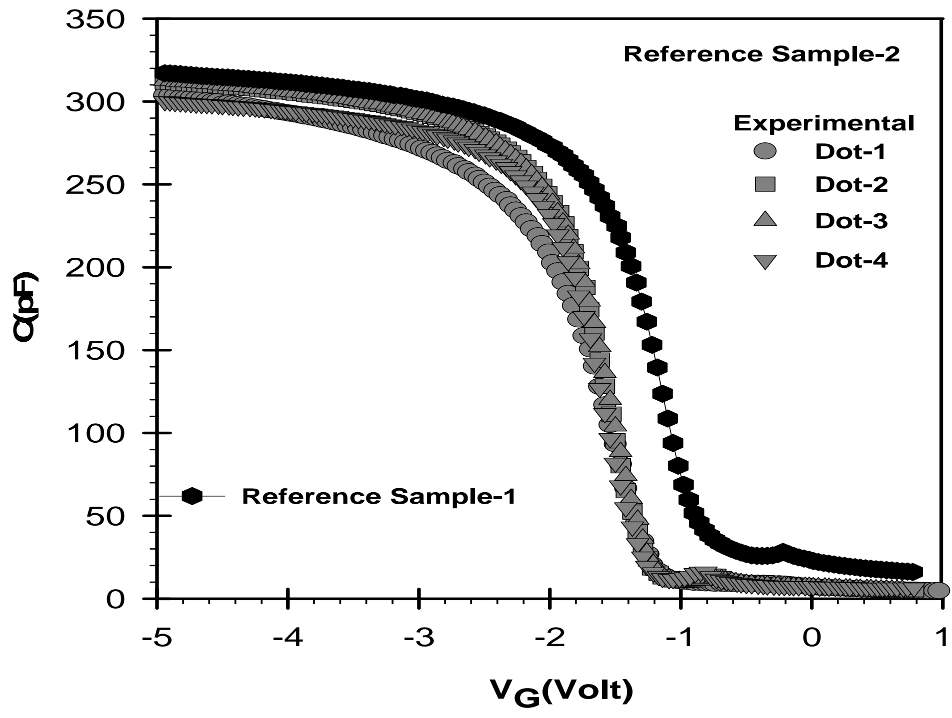


Figure 4.8. High frequency capacitance versus gate voltage curves of Al-Ta_2O_5-(SiO_2)-Si MOS capacitors

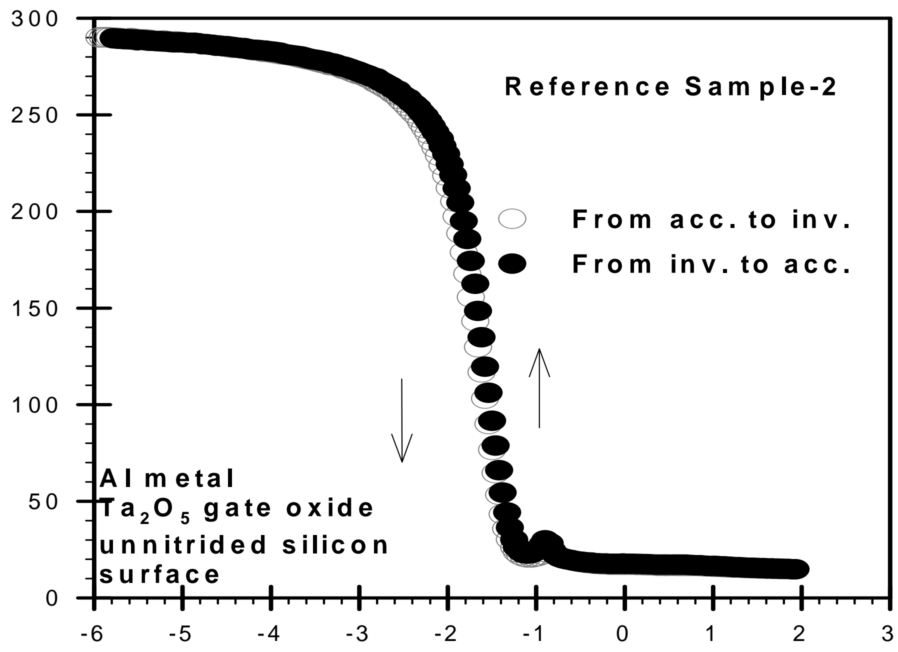


Figure 4.9. Forward and reverse C-V curve of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor with unnitrided Si surface

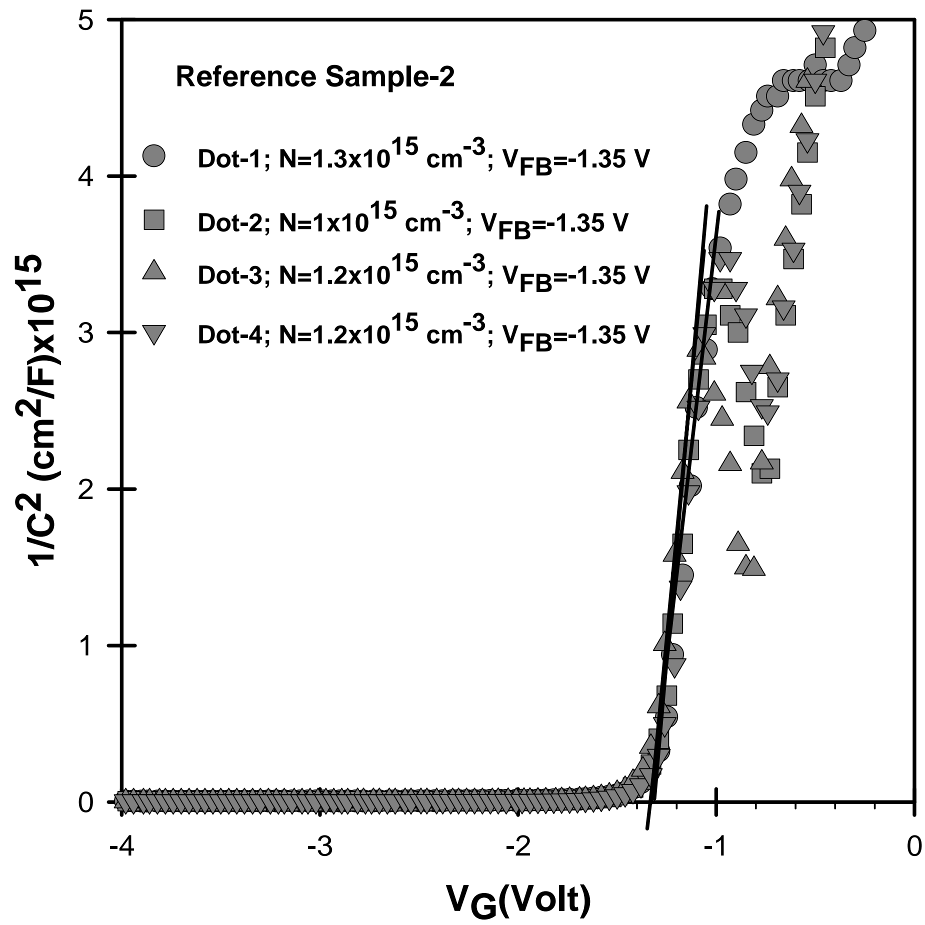


Figure 4.10. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of $Al-Ta_2O_5-(SiO_2)-Si$ MOS capacitor

is $1.2\pm0.1x10^{15}$ cm^{-3} and flat band voltage V_{FB} is around -1.35 V as obtained from the intercept on V_G axis. Higher flat band voltage shift to negative voltages indicates higher density of effective oxide charges present in high-k Ta_2O_5 oxide layer, which is higher than that of reference sample-1 with native SiO_2.

The effect of high density effective oxide charges are clearly seen as the shift of experimental C-V curve from the theoretical one. In Figure 4.11, both calculated theoretical and experimental C-V curves normalized to oxide capacitance are shown for dot-1. It is clearly seen that substantial shift of experimental C-V curve from the ideal one indicates the higher level of effective oxide charges seen in high-k oxide layers. In addition simultaneously measured conductance versus gate voltage V_G measured at 1MHz for the same dot is also presented in Figure 4.11, indicating a peak value around V_{FB} voltage of the experimental C-V curve, which is a further confirmation for V_{FB} voltage. For this sample, due to the high concentration of the electrically active defect located inside the bulk of the insulating layer, the obtained conductance values are around 90 μS which is almost four times higher than that of SiO_2. On the other hand, using the V_{FB} flat band voltage shifts of each dot, the density of effective oxide charges, N_{eff} present in Ta_2O_5 oxide layer have been calculated for each dot shown in Figure 4.8. It was found that $N_{eff}=3.2x10^{12}$ cm^2, which is substantially higher than that of reference sample-1 with native oxide SiO_2. Current density J versus gate voltage V_G curve of the same dot-1 is shown in Figure 4.12 for both reference sample -1 and reference sample-2. It is clearly seen that MOS capacitor with Ta_2O_5 has higher leakage current than that of native SiO_2, which is the main problem of high-k dielectrics.

Another important issue of MOS capacitors with high-k oxide layer formed on silicon surface is the quality of Si-Ta_2O_5 interface. Due to thermodynamic instability between silicon and Ta_2O_5 oxide layer, there is no good quality interface formed between silicon and Ta_2O_5 oxide layer. Generally not well defined interface is formed and density of ınterface sates become higher than that of Si-SiO_2 interface. In order to determine the levels of interface states, surface voltage ψ_s versus gate voltage V_G curves have been calculated and shown in Figure 4.13 for each dot. Finally, D_{it} levels versus energy for reference sample-2 are shown in Figure 4.14. It is clearly seen that D_{it} levels for reference sample-2 with Ta_2O_5 is almost equal to (11 ± 2) $x10^{11}(eVcm^2)^{-1}$ and is almost one order of magnitude higher than that of reference sample-1, indicating lower quality of Si-Ta_2O_5 interface. Average value of D_{it} levels of four different dots of

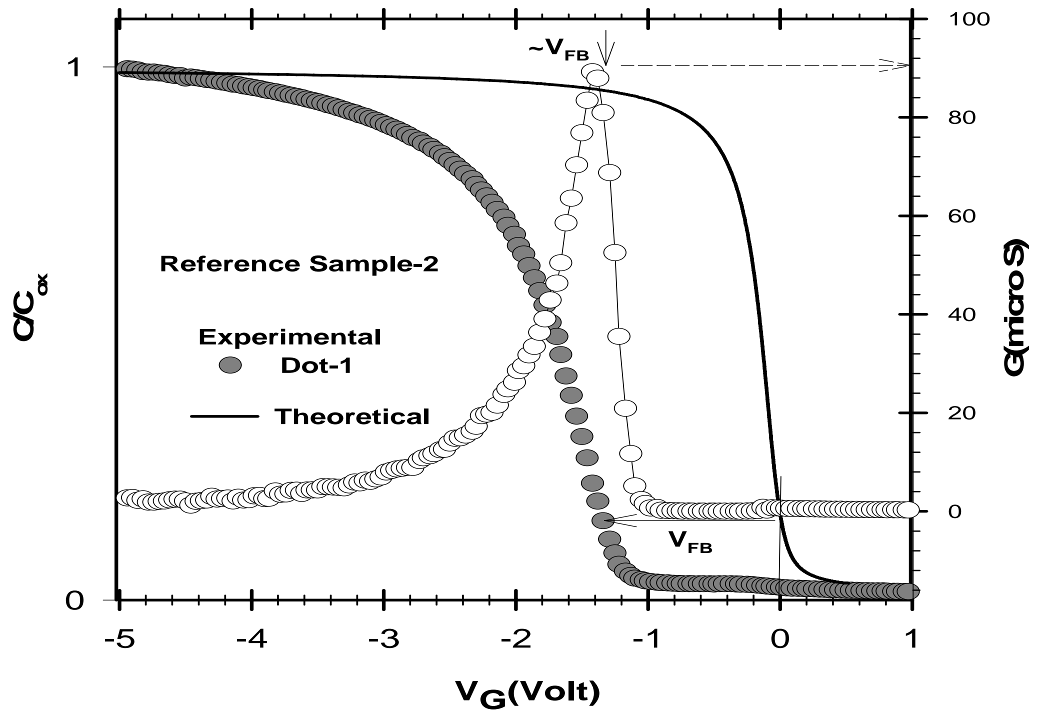


Figure 4.11. Normalized experimental and theoretical capacitance versus gate voltage and conductance versus gate voltage of Al-Ta_2O_5-Si MOS capacitor

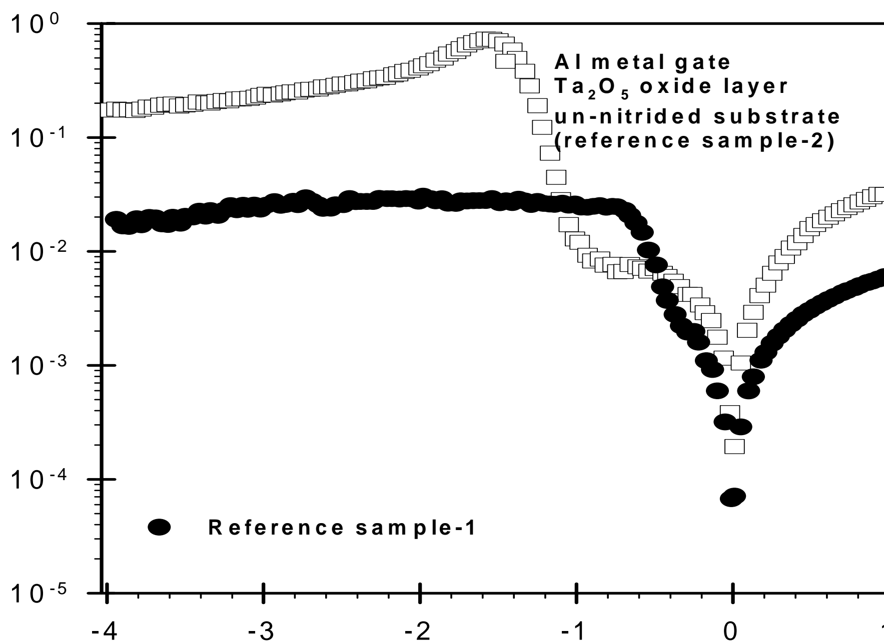


Figure 4.12. J-V characteristics of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor, reference sample-2 and reference sample-1.

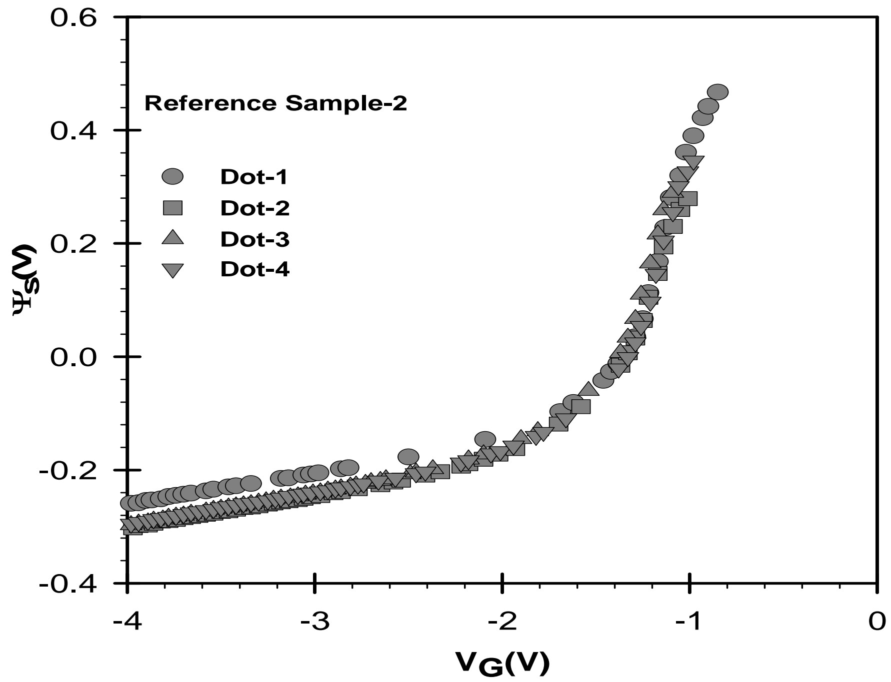


Figure 4.13. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox}-V curves of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor

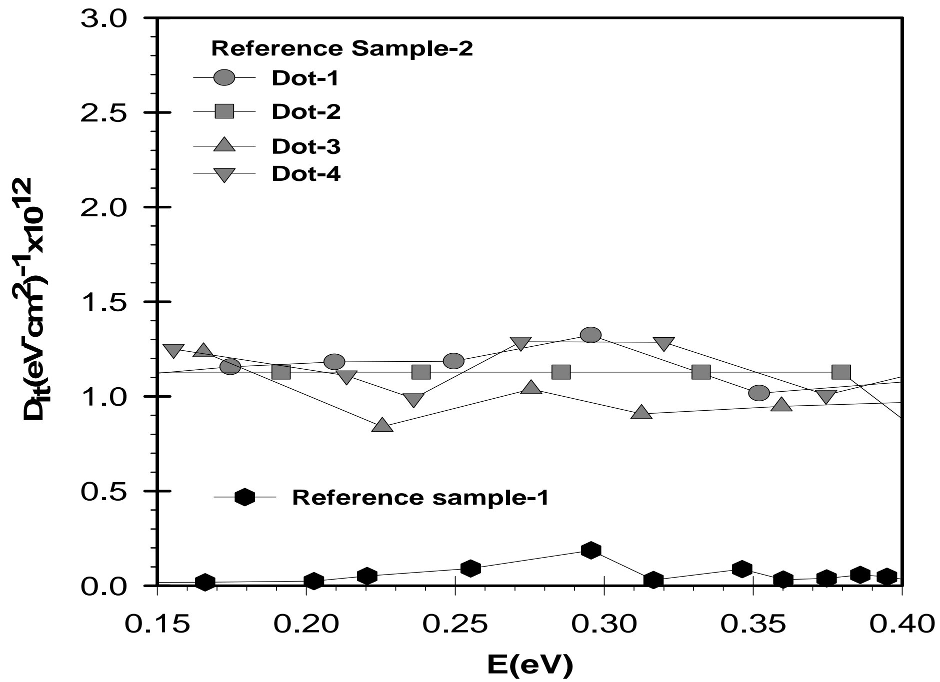


Figure 4.14. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor.

reference sample-2 are also summarized in Table 4.2. Even though an increase in dielectric constant is obtained for Ta_2O_5 oxide layer, its oxide quality and interface quality between Si-Ta_2O_5 is much below than that of native oxide SiO_2 and Si-SiO_2 interface, respectively.

Table 4.2. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_2)-Si MOS capacitor prepared without nitridation

<table>
<tr><th>Dot</th><th>t_{ox} (nm)</th><th>S (cm2)</th><th>k</th><th>C_{ox} (pF)</th><th>Na (cm^{-3}) $x10^{15}$</th><th>V_{FB} (slope) (volt)</th><th>V_{FB} (shift) (volt)</th><th>t_{eq} (nm)</th><th>N_{eff} $x10^{11}$ (cm^{-2})</th><th>D_{it} $x10^{11}$ ($eVcm^2)^{-1}$</th></tr>
<tr><td>Dot-1</td><td rowspan="4">20</td><td rowspan="4">6.25 $x10^{-4}$</td><td>11</td><td>303</td><td>-1.3</td><td>-1.35</td><td>-1.4</td><td>7</td><td>32</td><td>11.5±2</td></tr>
<tr><td>Dot-2</td><td>11.2</td><td>311</td><td>-1.3</td><td>-1.35</td><td>-1.4</td><td>6.9</td><td>32</td><td>11.1</td></tr>
<tr><td>Dot-3</td><td>10.8</td><td>300</td><td>-1.3</td><td>-1.35</td><td>-1.4</td><td>6.9</td><td>32</td><td>10±2</td></tr>
<tr><td>Dot-4</td><td>11.3</td><td>312</td><td>-1.2</td><td>-1.35</td><td>-1.4</td><td>6.8</td><td>32</td><td>11±2</td></tr>
</table>

4.4 The Effect of Prior Nitridation of Silicon Surface

In this thesis, the effect of a prior nitridation process of silicon surface before Ta_2O_5 oxide formation in MOS capacitors have been investigated using high frequency C-V method. Nitridation process has been carried out under N_2O and NH_3 gas ambients at temperature between 700 ^oC and 850 ^oC. The results of Al-Ta_2O_5-(SiO_xN_y)- Si MOS capacitor, prepared using different nitridation process will be presented and compared with reference samples.

In order to improve leakage currents through the oxide, effective oxide charges and Si-Ta_2O_5 interface properties, interface treatment method called Rapid Thermal Nitridation (RTN) has become one of the most attractive methods in MOS fabrication process. Nitridation process is commonly used to passivates Si surface from the oxide layer and improve the interface properties between Si-Ta_2O_5.

4.4.1 Prior Nitridation of Silicon Surface in N_2O Gas Ambient

Prior nitridation process of silicon surface has been carried out in N_2O gas environment at 700ºC, 800ºC and 850ºC before Ta_2O_5 oxide formation. After Al evaporation, MOS capacitor were prepared and characterized. In the following, first the results of MOS capacitors with 700 º C nitridation processes will be presented and compared with previous reference samples. Then, the result of 800ºC and 850ºC nitridation process will be presented. An interfacial silicon oxynitride layer with thickness of 1.5 nm has been formed in N_2O gas environment.

Experimental capacitance-voltage characteristics of four different MOS capacitors obtained from the same substrate are shown in Figure 4.15 for nitridation process at 700ºC in N_2O gas ambient. From the accumulation region, the oxide capacitance values were measured to be 185 pF for all samples. The oxide thickness was 20 nm and the surface area of metal gate was $6.25x10^{-4}$ cm^{-2}. Calculated dielectric constant is around 6.9 for different dots, which is smaller than reference sample-2. The equivalent oxide thickness of SiO_2, which gives the same capacitance value as obtained for this sample is found to be 11 nm.

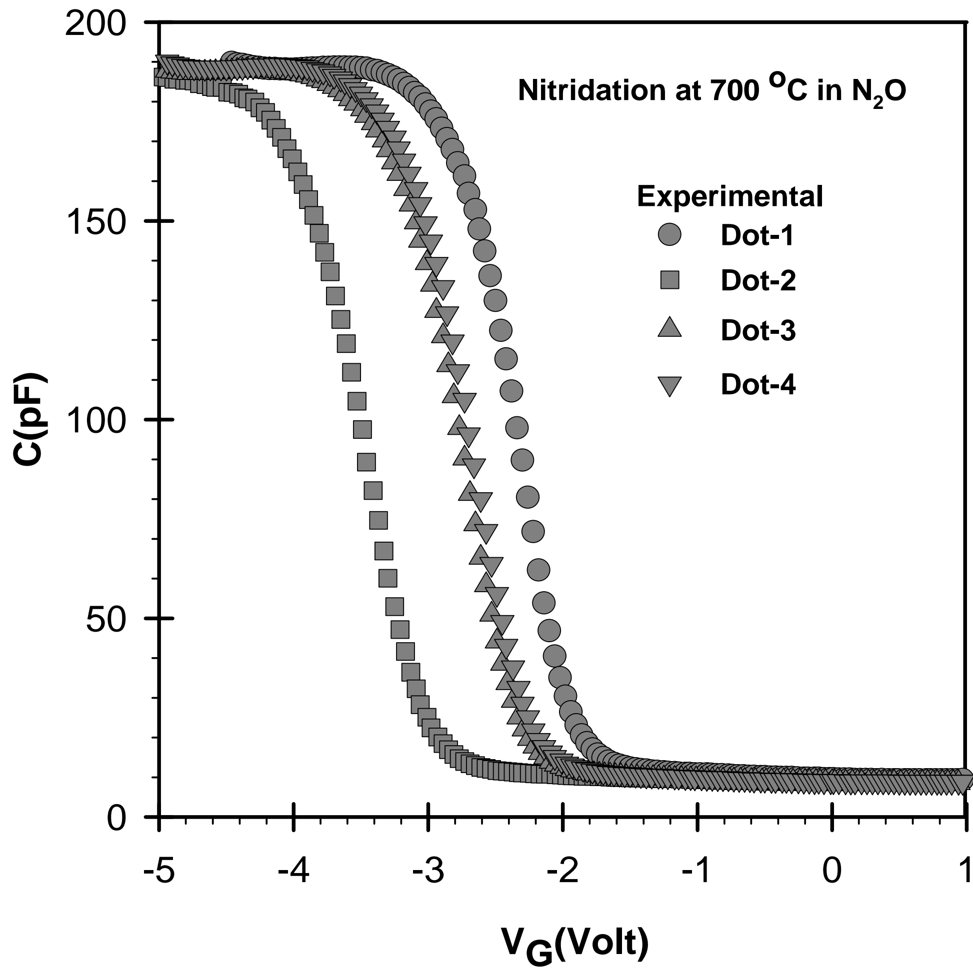
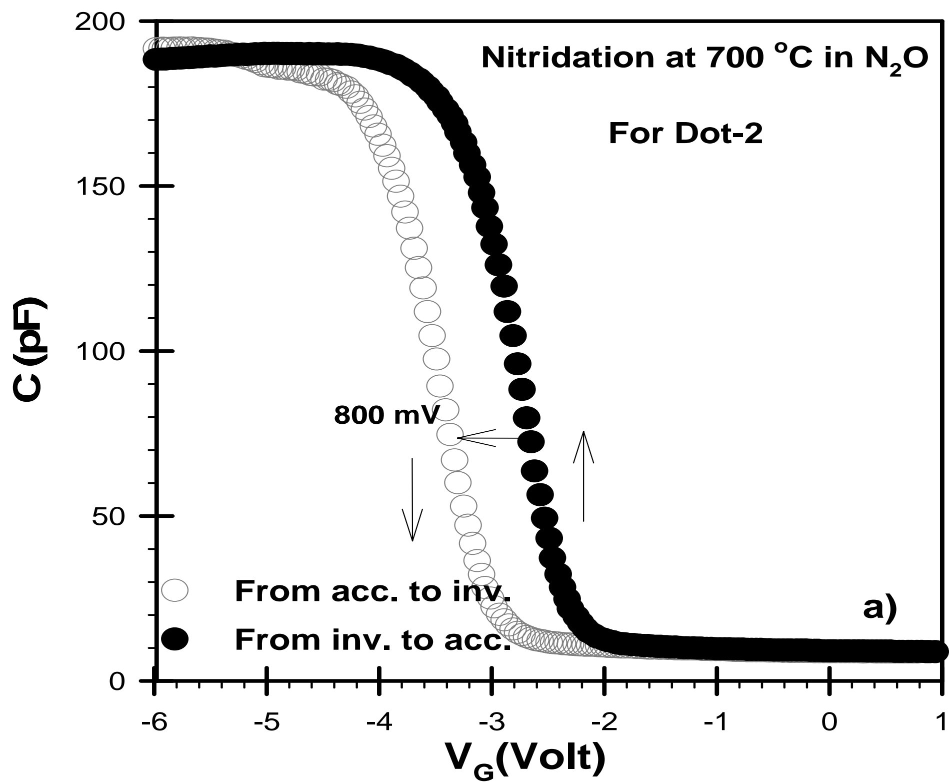


Figure 4.15. High frequency capacitance versus gate voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors for nitridation temperatures at 700 °C in N_2O gas environment.

Hysteresis effect in high frequency C-V measurements shows variation among the samples measured from the same substrate. In Figure 4.16, two different hysteresis curves were shown for two different dots taken from the same substrate. All samples exhibit counterclockwise hysteresis, however, the ΔV_{FB} voltage shifts varies between 30 mV and 800 mV among the dots, indicating different mobile trapped charges acting in different dot. The corresponding positive mobile trap charge for these voltage shifts are calculated with the help of equation 3.30 as 5.97×10^{10} cm^{-2} and 1.52×10^{12} cm^{-2}, respectively.

Doping concentration N_A and V_{FB} flat band voltage shifts were obtained from $1/C^2$ versus V_G curves shown in Figure 4.17. Even though N_A is almost identical for all samples, the V_{FB} voltage shifts are different for each dot. It indicates that there is a variation in N_{eff} as well. This is clearly seen as the ideal C-V is calculated for each sample and presented together with experimental data. In Figure 4.18, both ideal and experimental C-V curves normalized to oxide capacitance C_{ox} are shown for dot-1 together with high frequency conductance versus gate voltage V_G curve. A large shift of V_{FB} to negative voltage is also consistent with the peak position of conductance curve of the same sample. Similar consistent agreements have been obtained for other dots between V_{FB} shift of C-V and conductance curve. However, this sample shows substantially high conductance values around 330μS even higher than that of reference sample-2. The density of effective oxide charge, N_{eff}, was calculated using the V_{FB} voltage shift obtained from ideal and experimental C-V curves. The values of Neff vary between 3×10^{12} cm^{-2} and 5×10^{12} cm^{-2} among the dots. The level of N_{eff} is still high, same as that of reference sample-2. There is no improvement in N_{eff} due to the nitridation in N_2O at 700 ^oC. However, leakage current characteristic of one of the samples shown in Figure 4.19 indicates good improvement as compared to reference sample-1.

The major effect of prior nitridation process is to improve $Si\text{-}Ta_2O_5$ interface by forming a few nm SiO_xN_y layer at the interface. Dit level, calculated from the ψ_s versus V_G data shown in Figure 4.20 are presented in Figure 4.21. It is a clear indication that interface quality between silicon and Ta_2O_5 has been substantially improved and D_{it}



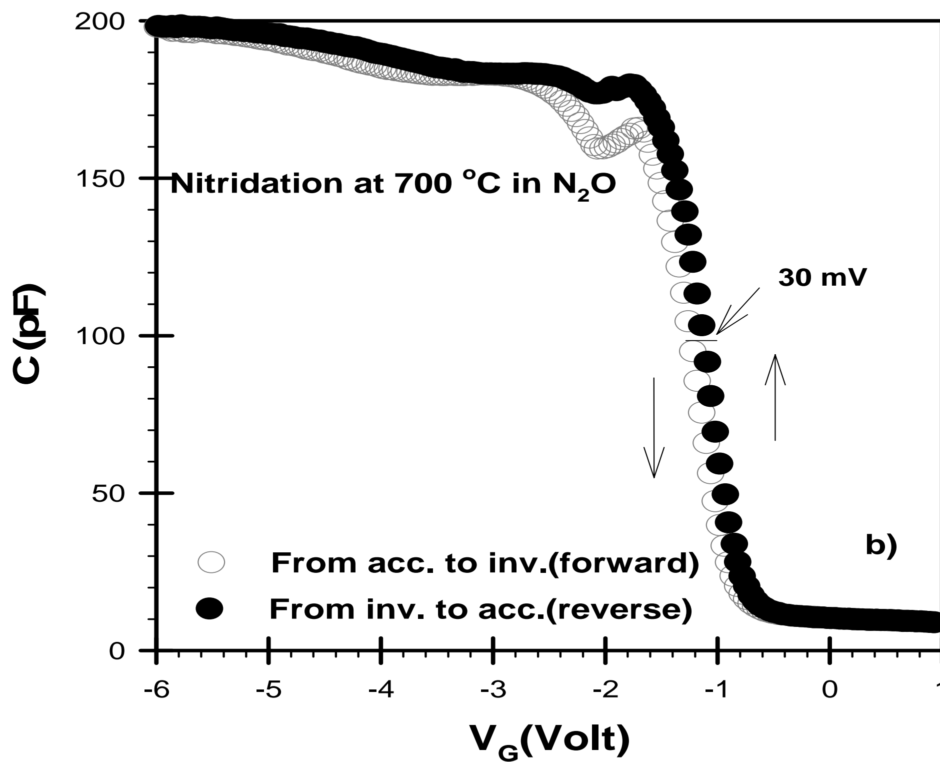


Figure 4.16. Forward and reverse C-V curve of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor with nitrided Si surface at 700 °C in N_2O for two MOS capacitor obtained on the same substrate

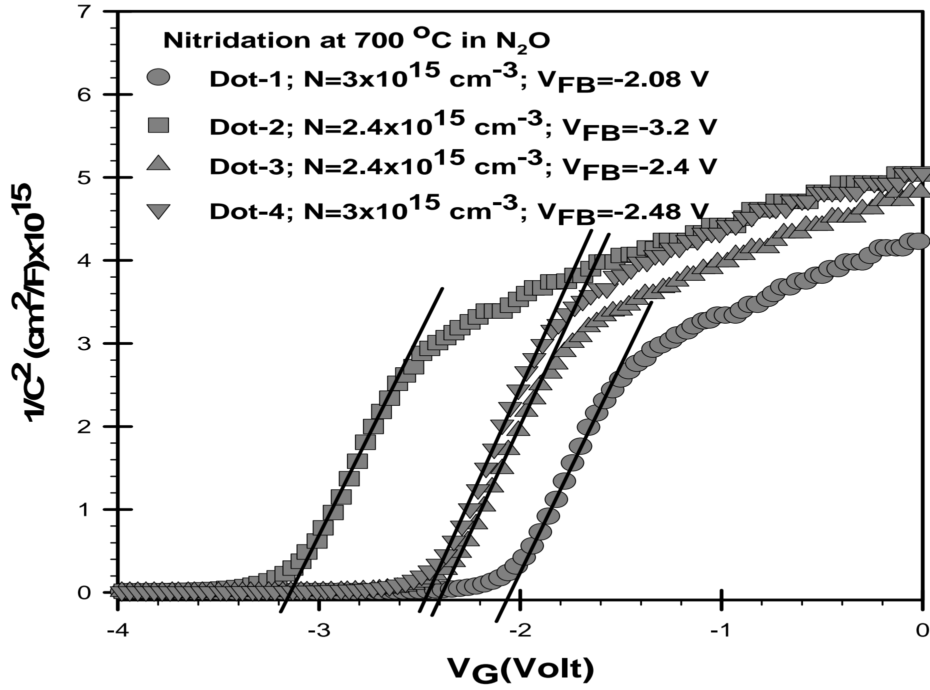


Figure 4.17. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation temperature at 700 °C in N_2O gas environment

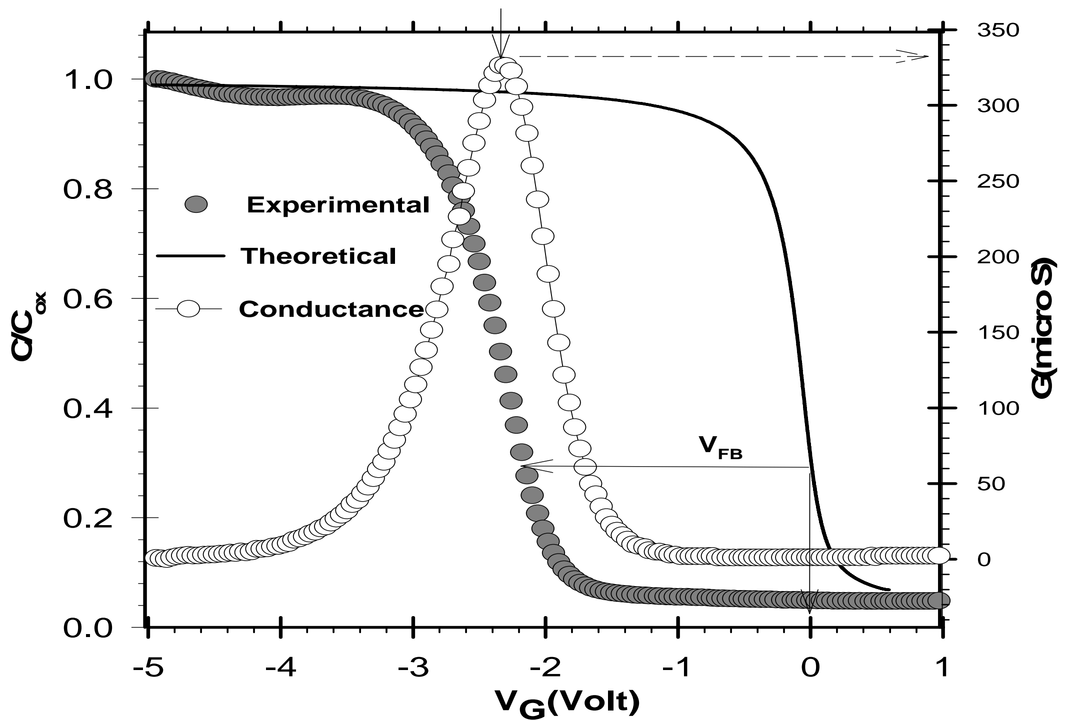


Figure 4.18. Normalized experimental and theoretical capacitance versus gate voltage and conductance versus gate voltage of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 700ºC.

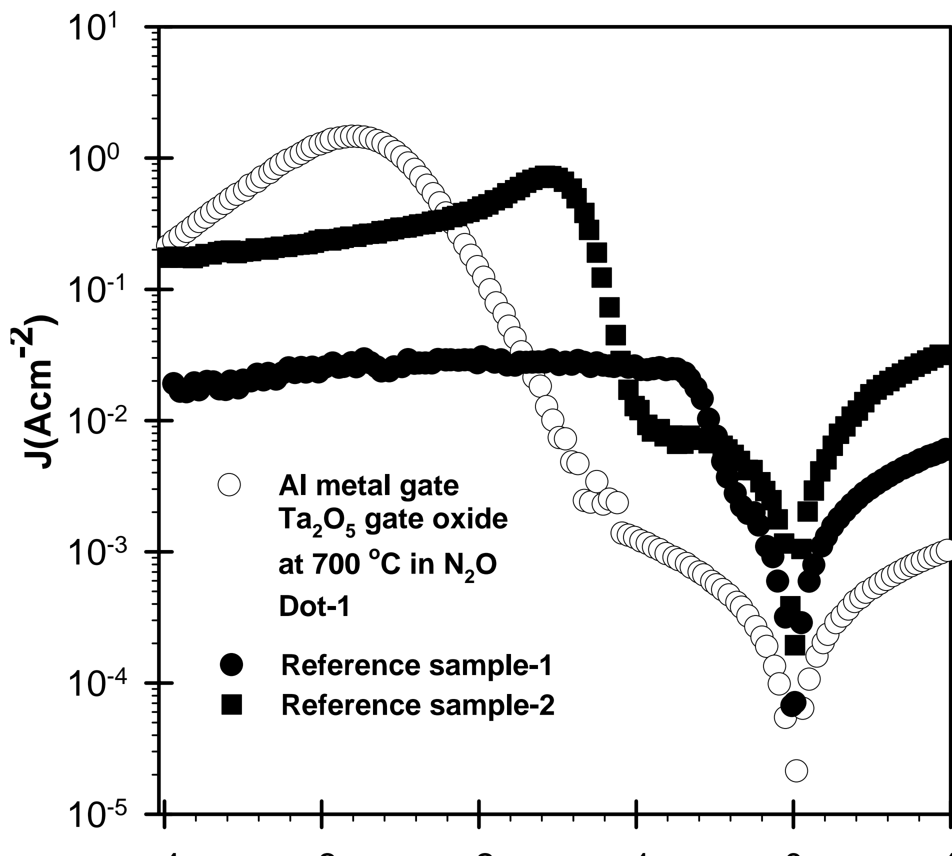


Figure 4.19. J-V characteristics of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 700 ^oC in N_2O and that of the reference sample-1.

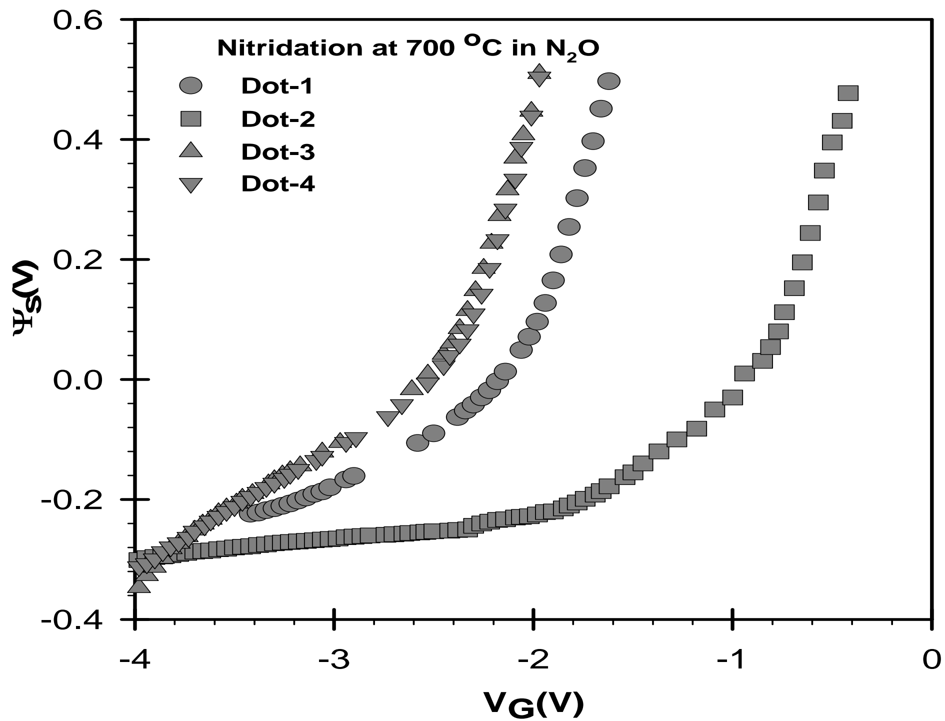


Figure 4.20. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox}-V_G curves of reference samples-1,2 and Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 700ºC

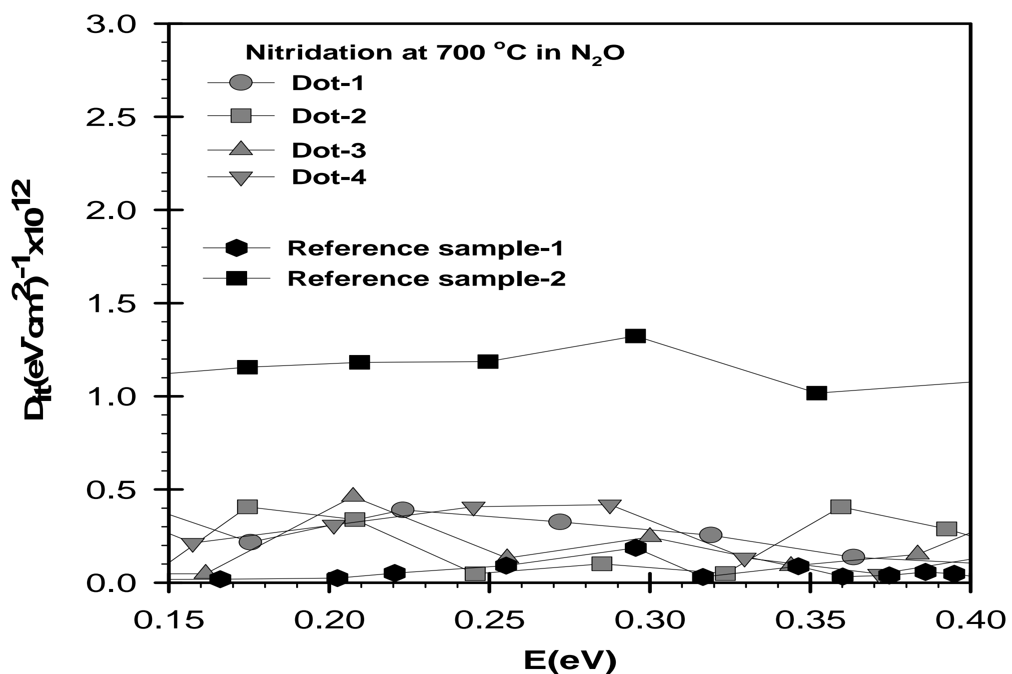


Figure 4.21. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at 700ºC.

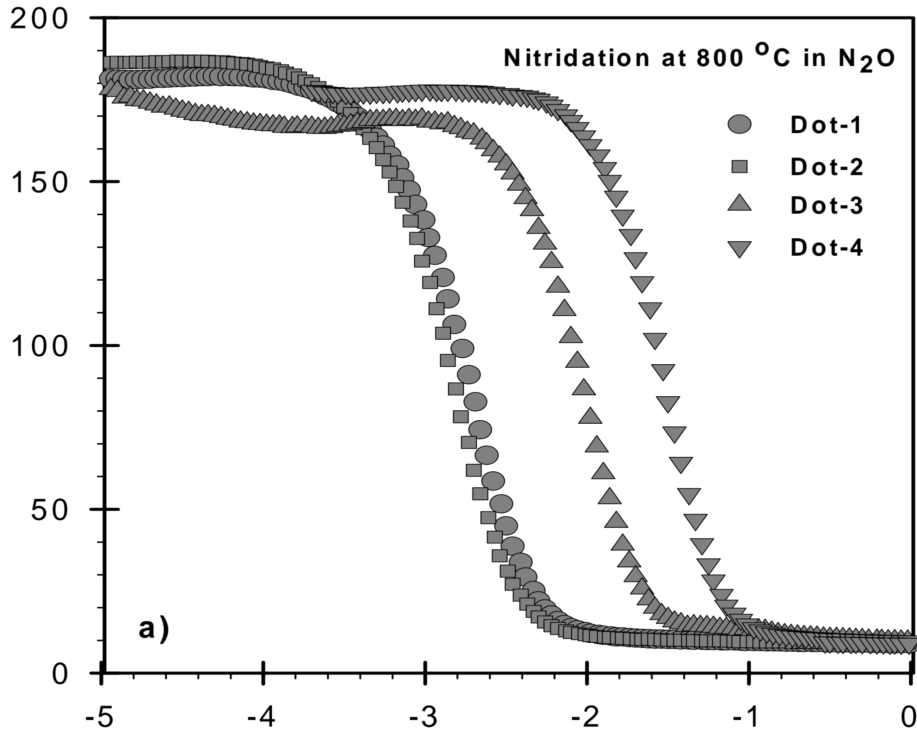
level decreased to the levels of reference sample-1 and reach the value of $3\pm1x10^{11}$ $(eVcm^2)^{-1}$ as summarized in Table 4.3. D_{it} level was an order of magnitude higher for reference sample-2, with Ta_2O_5 oxide layer formed on unnitrided silicon surface.

Table 4.3. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 700 ^oC in N_2O gas ambient

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) $x10^{15}$	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} $x10^{11}$ (cm^{-2})	D_{it} $x10^{11}$ $(eVcm^2)^{-1}$
Dot-1	20	6.25 $x10^{-4}$	6.9	190	-2.4	-2.08	-2.1	11.3	32	3 ± 1
Dot-2			6.9	189	-2.4	-3.2	-3.3	11.4	50	3 ± 1
Dot-3			6.7	187	-2.4	-2.4	-2.6	11.5	29	2 ± 2
Dot-4			6.9	190	-3	-2.5	-2.5	11.3	32	3 ± 1

It was shown that nitridation of Si surface in N_2O gas ambient at 700ºC has greatly improved the interface quality between silicon and Ta_2O_5 insulating layer. Nitridation in N_2O gas have also been carried out at 800ºC and 850ºC. For both process temperature, the results of four different dots from the same substrate show almost identical oxide capacitance values as shown in Figure 4. 22. For nitridation process at 800ºC, dielectric constant obtained from oxide capacitance measured at accumulation is almost the same as that found for nitridation process at 700ºC, which is around 6.5. However it increases to 10.2 for nitridation process carried out at 850ºC. Moreover, the equivalent oxide thickness t_{eq} of SiO_2 which gives the same capacitance values are obtained to be 11 nm for nitridation process at 800ºC, while 7.6 nm for nitridation process at 850ºC.

Hysteresis behaviors of the samples were also measured. It was found that hysteresis behavior of the high frequency C-V curve is 700 mV for 800ºC sample and 600 mV for 850 º C sample as shown in Figure 4.23. Both of them indicate counterclockwise hysteresis, which is the result of a voltage shift towards negative voltages. These voltage shifts are similar to those found for the samples of nitridation



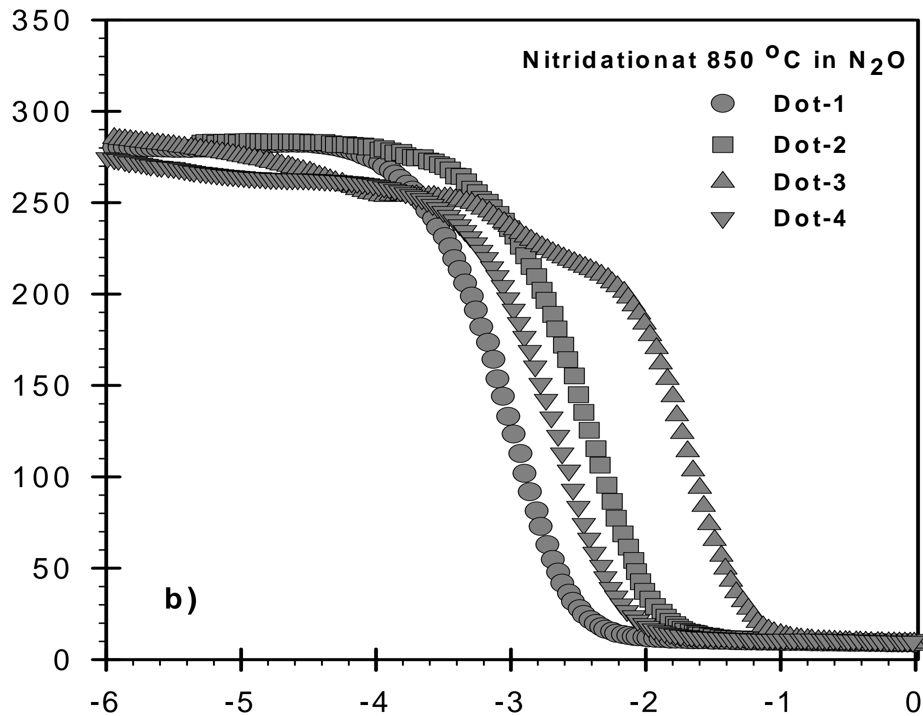
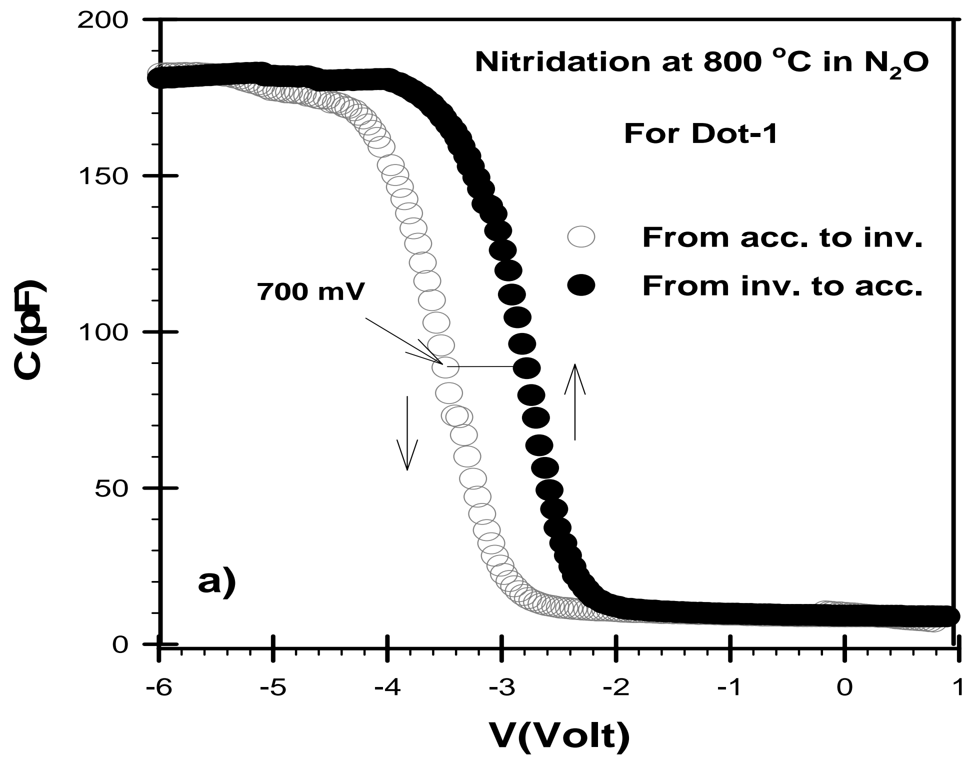


Figure 4.22. Experimental high frequency capacitance-voltage curves of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at a) 800ºC, b) 850ºC



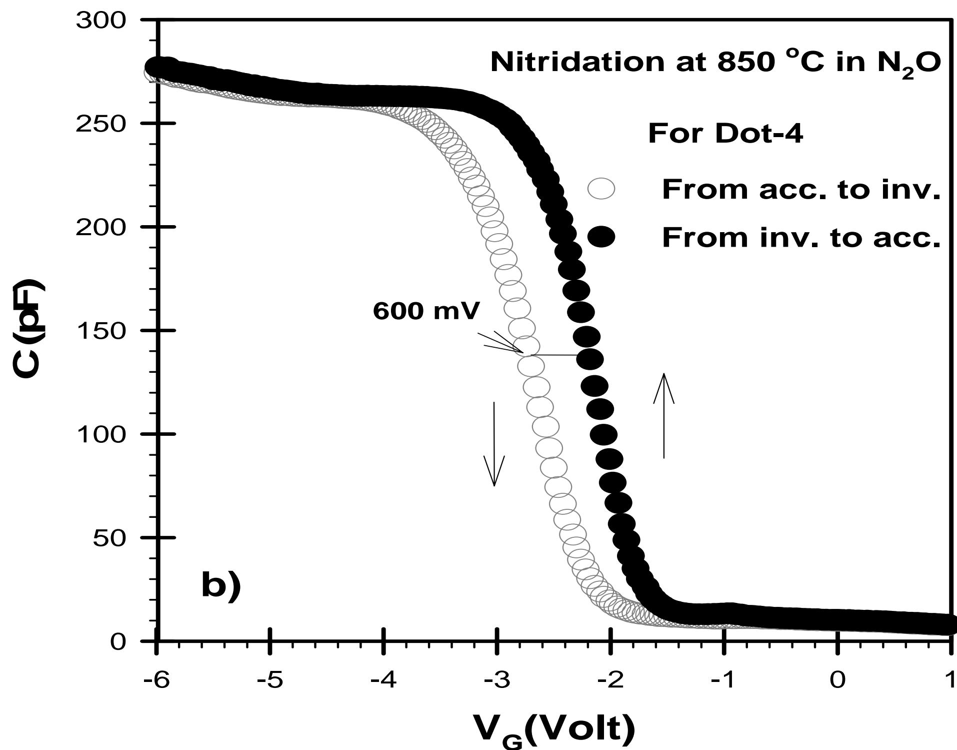
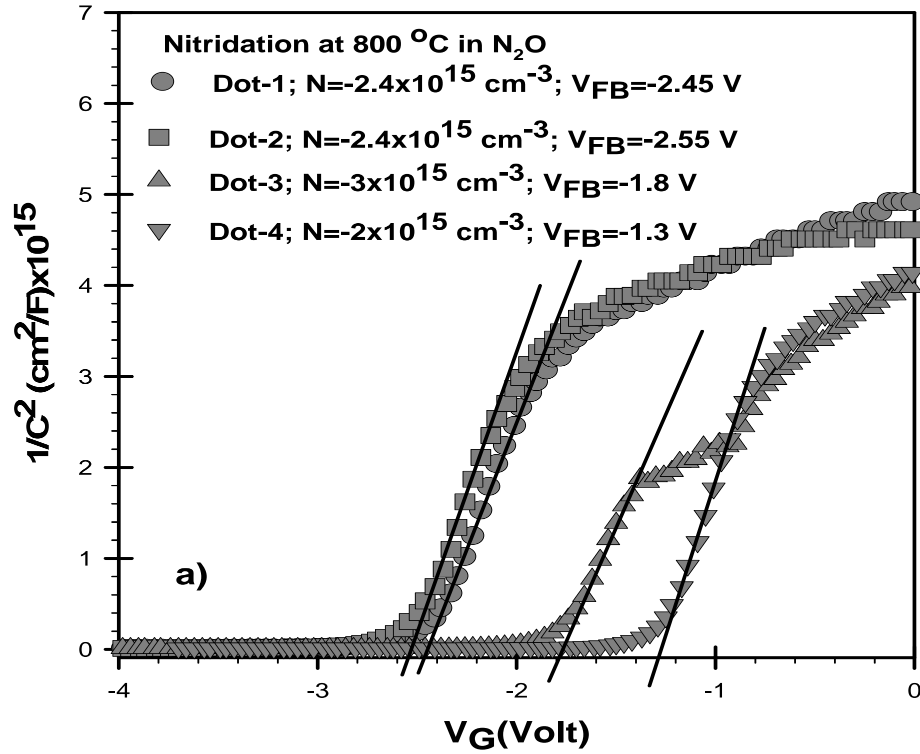


Figure 4.23. Forward and reverse C-V curve of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor with nitrided Si surface in N_2O at a) 800ºC, b) 850ºC

process at 700ºC. However, they are substantially higher than reference samples1, reference sample 2 and required levels of good quality high-k oxide layers. The corresponding positive mobile trap charge density for this voltage shift is calculated with the help of equation 3.29 as $1.27x10^{12}$ cm^{-2} for 800ºC process temperature and $1.72x10^{12}$ cm^{-2} for 850ºC process temperature, respectively.

Doping concentration N_A of silicon substrate and the flat band voltage V_{FB} shifts were obtained from $1/C^2$ versus V_G curves shown in Figure 4.24 for both process temperatures. N_A of the both samples shows almost identical values for each MOS capacitor obtained on the same substrate and found to be around $-2.4x10^{15}$ cm^{-3} for both temperature processes. However, the flat band voltage V_{FB} varies for each sample. The V_{FB} shift of each dot is consistent with that found from the peak position of conductance versus gate voltage as shown in Figure 4.25 for dot-1 of the sample at 800ºC and dot-3 at 850ºC. Comparing to sample obtained at 700 ºC higher conductance values were obtained for those samples. Moreover, as the nitridation temperature increased increase in conductivity of the insulating layer was observed. While maximum conductance values for the sample at 800 ºC is around 350 μS, it is around 400 μS for the sample at 850 ºC. Effective oxide charge density obtained from the voltage shifts indicate the levels of $(3\pm2)x10^{12}$ cm^{-2} for both 800ºC and 850ºC nitridation process in N_2O gas. This level of Neff is similar for nitridation at 700ºC and does indicate any improvement from that found in reference sample-1.

As the leakage currents concerned, for both 800ºC and 850ºC process samples shows lower leakage current at inversion region as shown in Figure 4.26. However, leakage current in the depletion region around flat band voltages V_{FB} of each sample are much higher than that of reference sample-1. This high level of leakage currents at V_{FB} voltage is consisted with peak value of conductance curve shown in Figure 4.25.



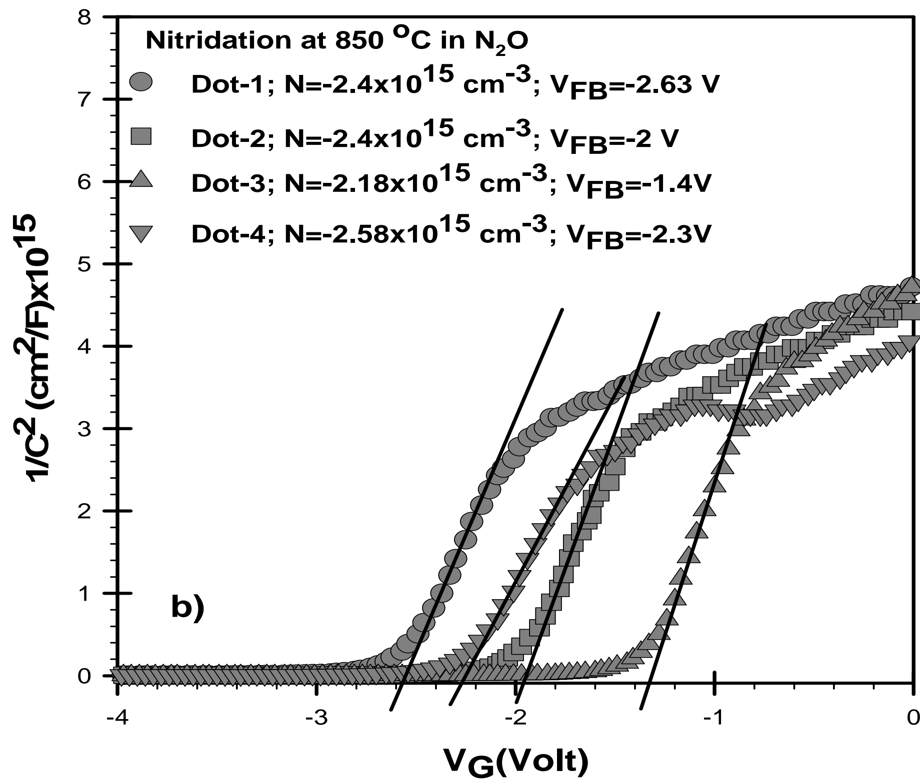


Figure 4.24. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation temperature at a) 800ºC b) 850ºC, in N_2O gas environment

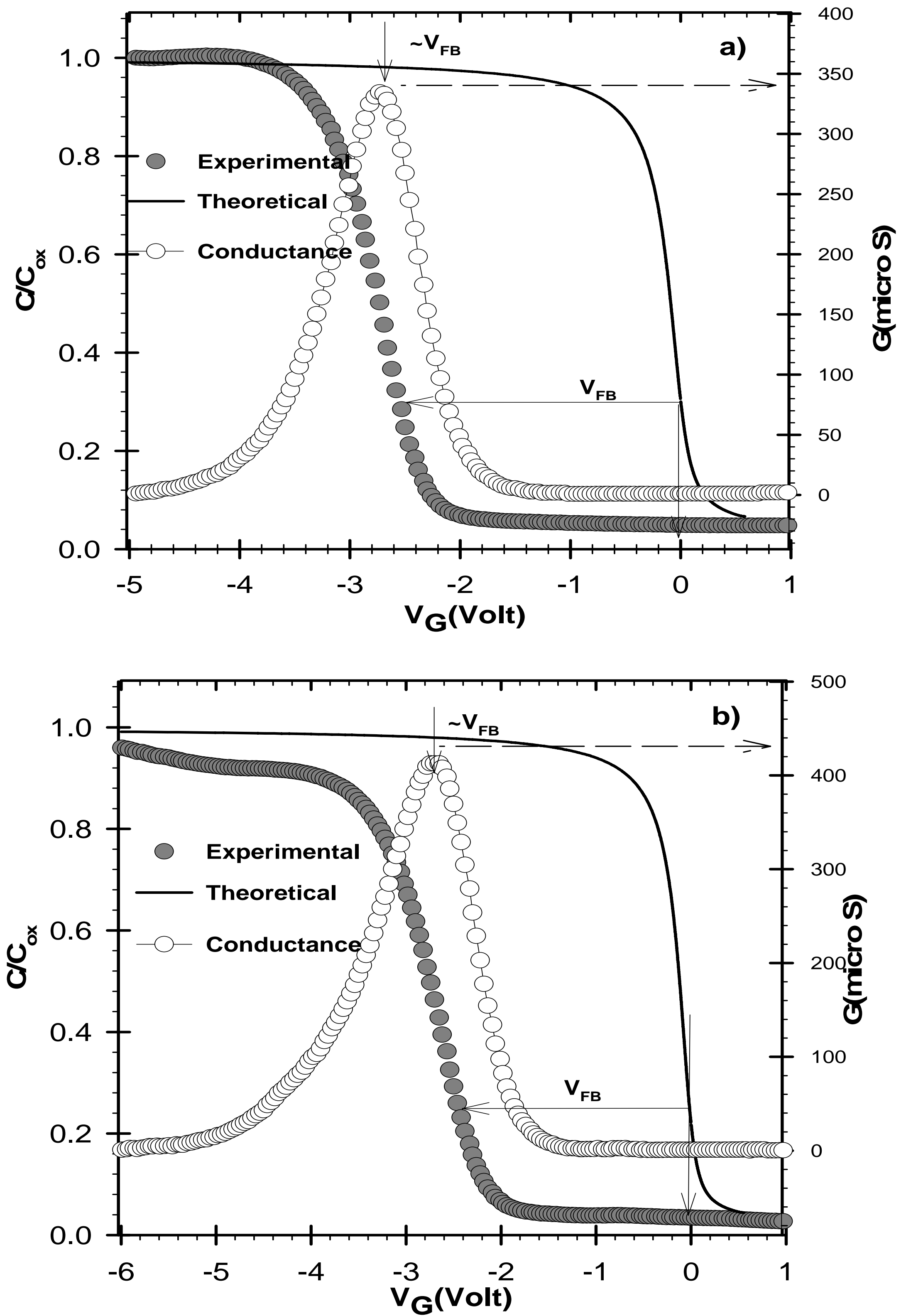


Figure 4.25. Normalized experimental and theoretical capacitance versus gate voltage and conductance versus gate voltage of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at a) 800ºC, b) 850ºC.

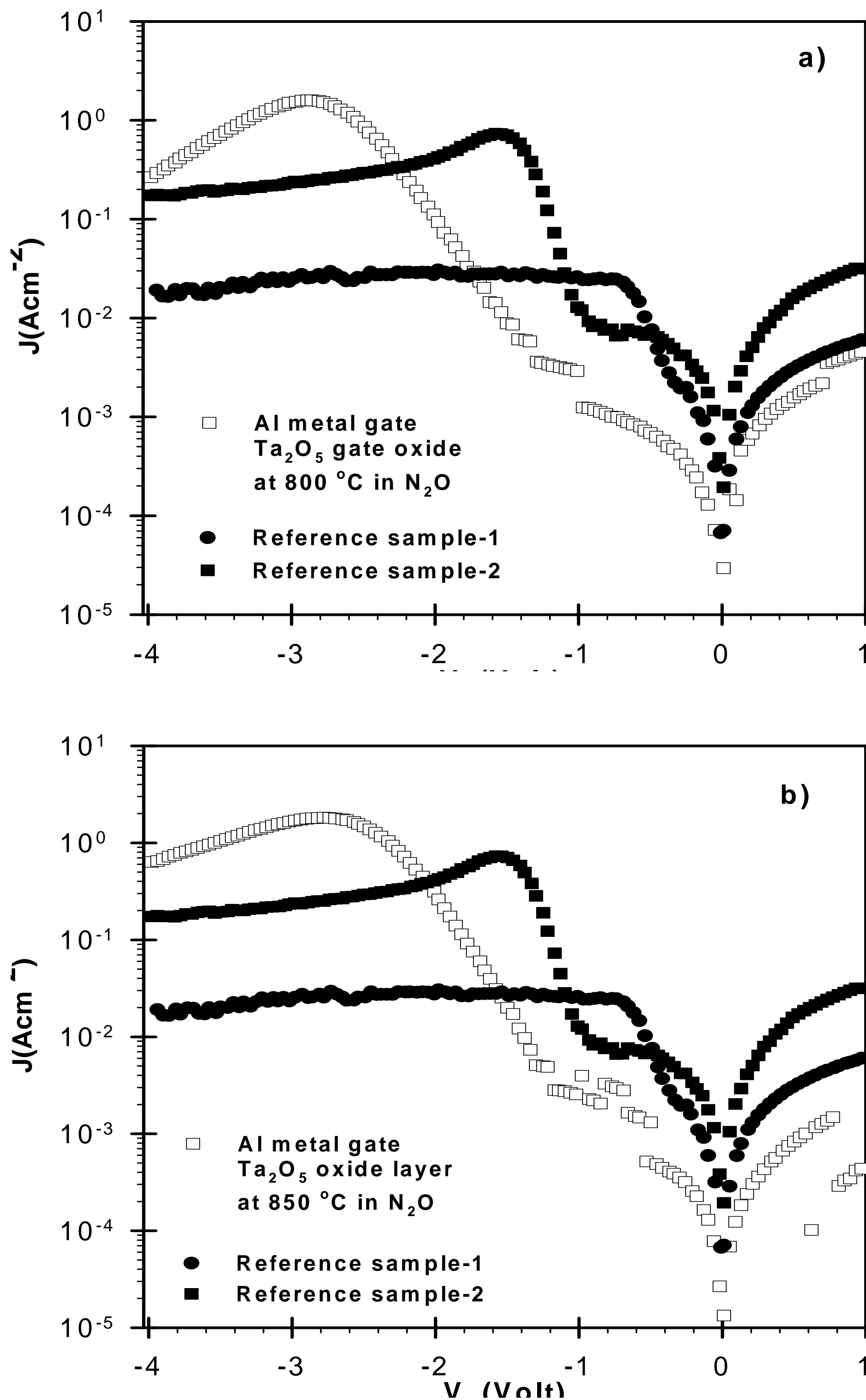
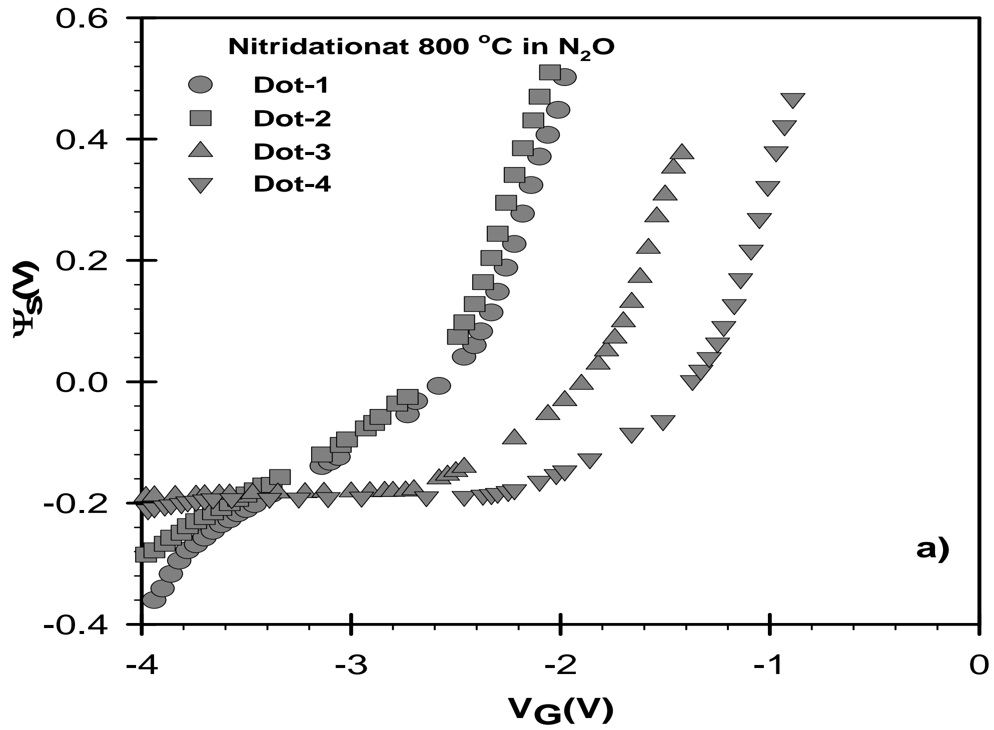


Figure 4.26. J-V characteristics of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at a) 800ºC, b) 850ºC, in N_2O with that of reference sample-1 and reference sample-2

Finally, the quality of $Si-Ta_2O_5$ interface after nitridation process at 800ºC and 850ºC was obtained from D_{it} levels calculated using Terman's method. ψ_s versus V_G curves obtained from normalized theoretical capacitance versus surface potential and normalized experimental high frequency capacitance versus gate voltage for both nitridation temperature are shown in Figure 4.27. From the data shown in Figure 4.27 the obtained D_{it} levels for both nitridation processes are shown in Figure 4.28 for every dot obtained on the same substrate. It is clearly seen that D_{it} levels are around $(3\pm1)x10^{11}$ $(eVcm^2)^{-1}$ for both group of dots. This level of D_{it} is very close to that of reference sample-1 with good quality interface formed by native oxide SiO_2. It can be concluded that nitridation of silicon surface before Ta_2O_5 formation has greatly improved the quality of $Si-Ta_2O_5$ interface for all nitridation temperature. This levels of D_{it} has decreased from $(11\pm2)x10^{11}$ $(eVcm^2)^{-1}$found for unnitrided reference sample-2 with the same quality Ta_2O_5 oxide layer. The extracted parameter from high frequency C-V measurement is shown in Table 4.4 and Table 4.5 for samples prepared with nitridation temperatures at 800 ^oC and 850 ^oC, respectively. It can be concluded that a prior nitridation of silicon surface before oxide formation has greatly improved the Si-Ta_2O_5 interface. However, the quality of oxide layer indicates higher levels of N_{eff} for all nitridation process temperatures. Among these three different nitridation temperatures, nitridation at 850 ^oC offers better dielectric constant of 10.3 and lowest equivalent oxide thickness values of 7 nm among other samples prepared with 700 ^oC and 800 ^oC.



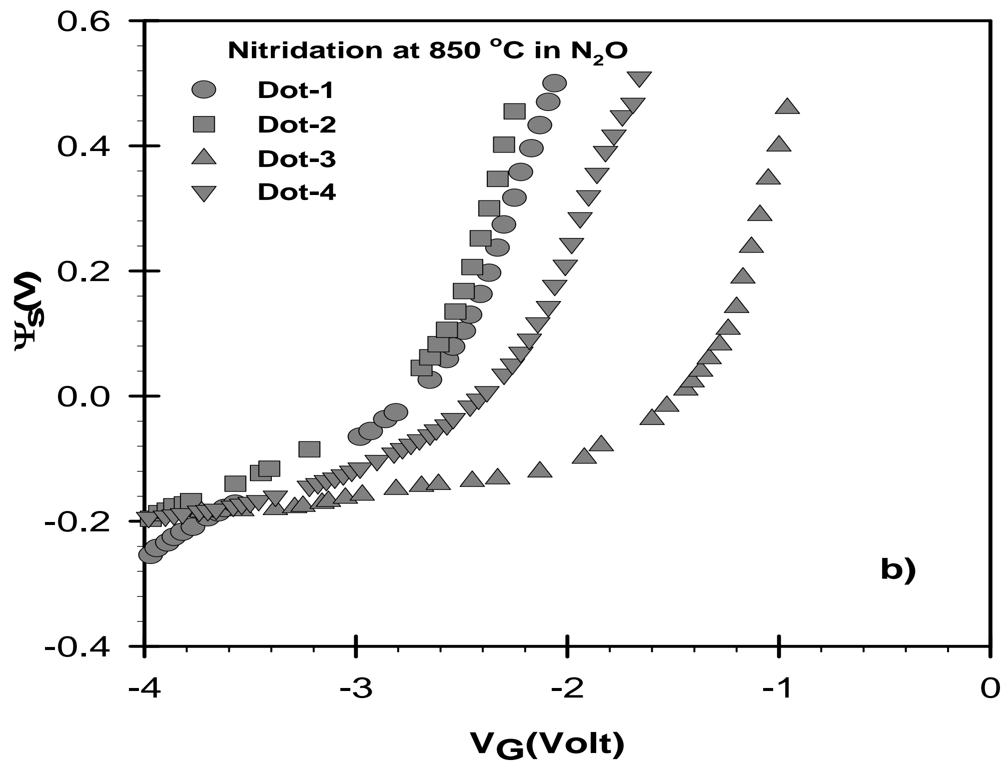
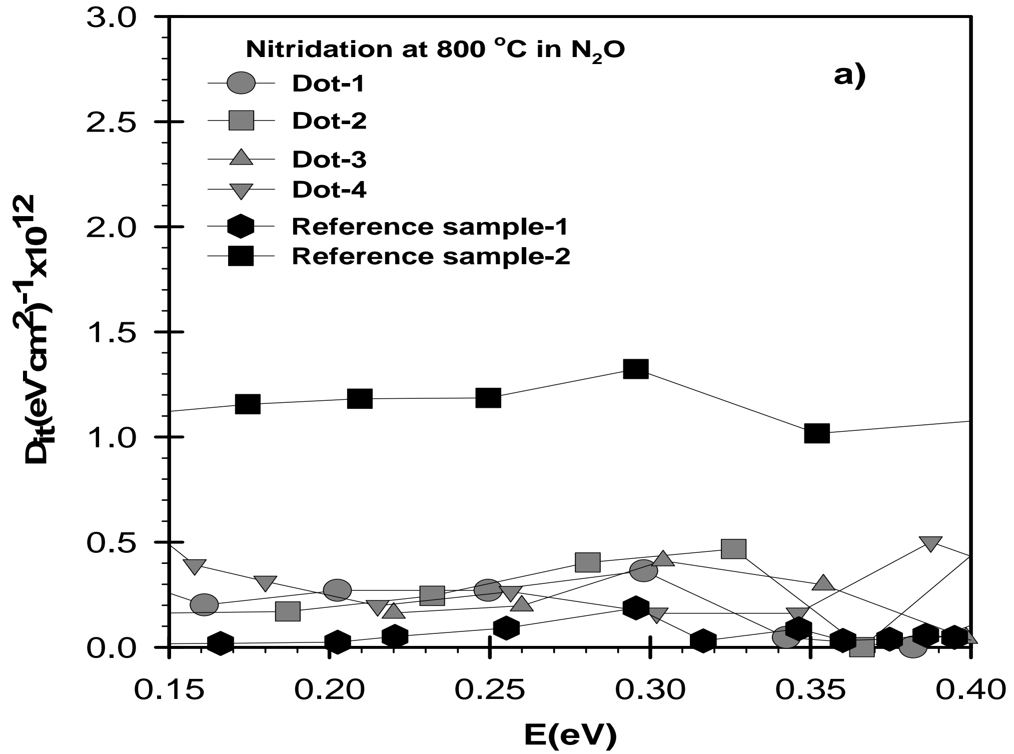


Figure 4.27. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox} vs V_G curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at a) 800ºC, b) 850ºC.



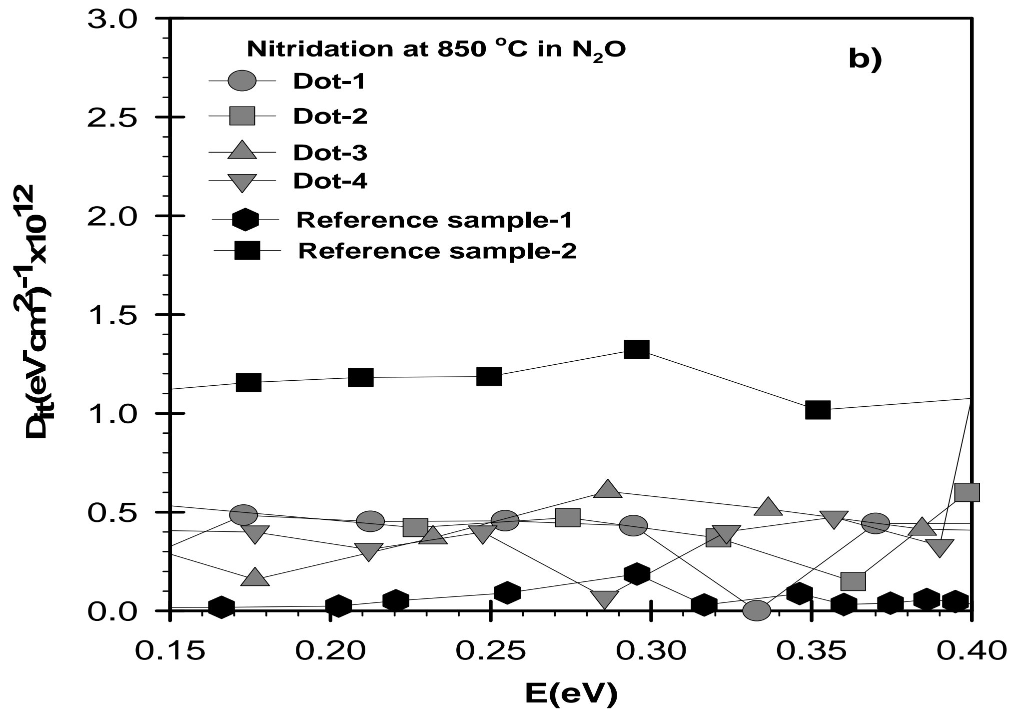


Figure 4.28. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at a) 800ºC, B) 850ºC with that of reference sample-1 and reference sample-2

Table 4.4. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 800ºC in N_2O gas ambient.

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (C-V shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} ($eVcm^2$)$^{-1}$
Dot-1	20	6.25 x10^{-4}	6.5	181	-2.4	-2.45	-2.6	11.3	40	3 ± 1
Dot-2			6.7	186	-2.4	-2.55	-2.7	11.4	42	2 ± 1
Dot-3			6.4	178	-3	-1.8	-1.9	11.5	29	2 ± 1
Dot-4			6.4	178	-2	-1.3	-1.4	11.3	18	2 ± 1

Table 4.5. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 850ºC in N_2O gas ambient.

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} ($eVcm^2$)$^{-1}$
Dot-1	20	6.25 x10^{-4}	10.2	280	-2.4	-2.63	-2.1	7.7	40	3 ± 1
Dot-2			10.2	282	-2.4	-2	-3.3	7.6	40	3 ± 1
Dot-3			10.3	285	-2.18	-1.4	-2.6	7.5	30	4 ± 2
Dot-4			10.3	286	-2.58	-2.3	-2.5	7.5	52	3 ± 1

4.4.2 Prior Nitridation of Silicon Surface in NH_3 Gas Ambient

As presented in previous section, nitridation process of silicon surface in N_2O gas prior to oxide formation has greatly improved the Si- Ta_2O_5 interface quality. Alternative nitridation process of silicon surface is carried out in NH_3 gas environment. In this thesis, electronic properties of metal-Ta_2O_5-SiO_xN_y-Si MOS capacitors were also investigated using a prior nitridation process of silicon surface in NH_3 gas environment at 700ºC and 800ºC.

High frequency C-V characteristics of MOS capacitors prepared after nitridation of silicon surface at 700ºC in NH_3 gas ambient are presented in Figure 4.29 for four different dots. It is seen that oxide capacitance at accumulation region shows slight variation around 335 pF±10 pF. This could be due to a strong interaction between gate metal and gate oxide Ta_2O_5, which causes slight differences in oxide thickness and capacitance values. In addition, oxide capacitance in accumulation region shows two step changes. These steps can be explained by trapping slow states. Dielectric constant was calculated for each sample by using oxide capacitance, measured oxide thickness and gate area of each sample. It is important that dielectric constant around 12 has been obtained for all samples, which is almost factor of 2 higher than that of samples nitrided in N_2O gas at the same temperature. It is a substantial improvement in dielectric constant for high-k oxide as compared to nitridation process carried out in N_2O gas.

The effects of mobile trap charges in oxide are presented in Figure 4.30 for Dot-3. Hysteresis effect of high frequency C-V curve shows 700 mV voltage shifts towards negative voltages. This indicates that positively charged mobile trap charges are present in Ta_2O_5 high-k oxide layer. Density of mobile trap charges is comparable to that observed in MOS capacitors prepared after nitridation process in N_2O gas at 700°C. Its density obtained from the voltage shift is in the range of $2.4x10^{12}$ cm^{-2}. Leakage current density versus gate voltage V_G obtained from the simultaneously measured conductance values is shown in Figure 4.31 for the capacitor presented as dot-3 of Figure 4.29. It is seen that leakage current density values are lower than that of reference sample-1 and reference sample-2 in inversion region. However, leakage currents of dot-3 in depletion region, at gate voltages around the V_{FB}, is higher than measured for reference sample-1 as seen in Figure 4.31.

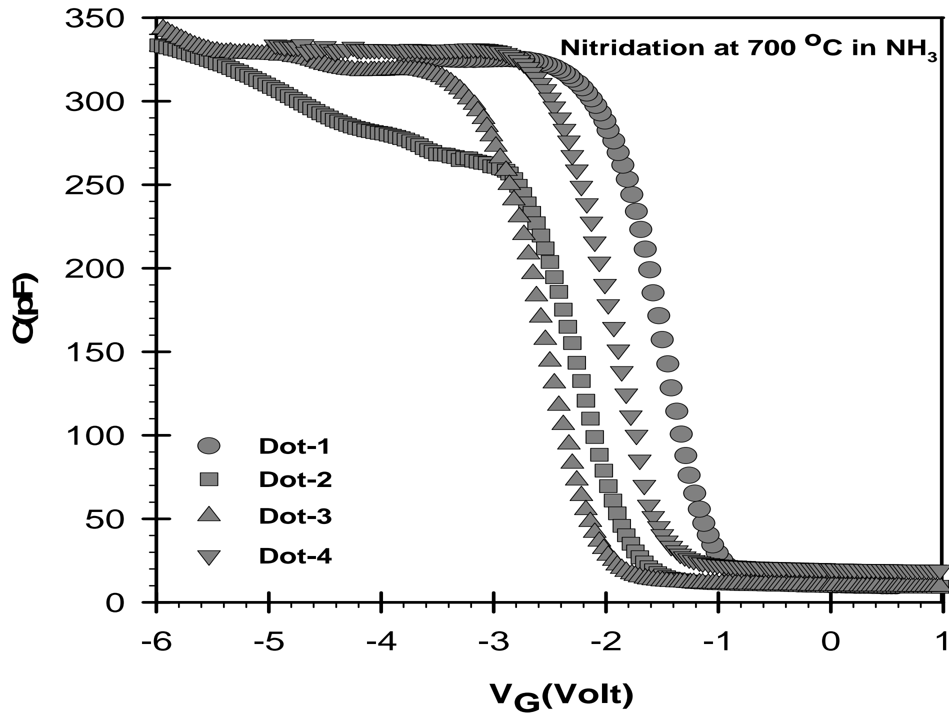


Figure 4.29. Experimental high frequency capacitance versus gate voltage curves of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process of silicon surface in NH_3 gas environment at 700ºC

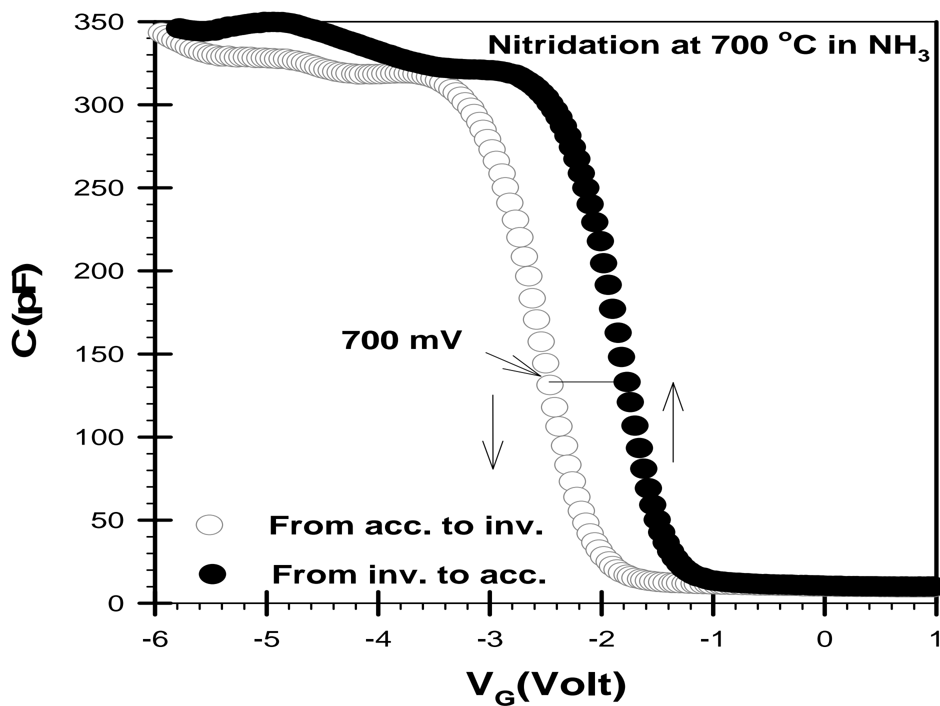


Figure 4.30. Forward and reverse C-V curve of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor with nitrided Si surface at 700ºC in NH_3

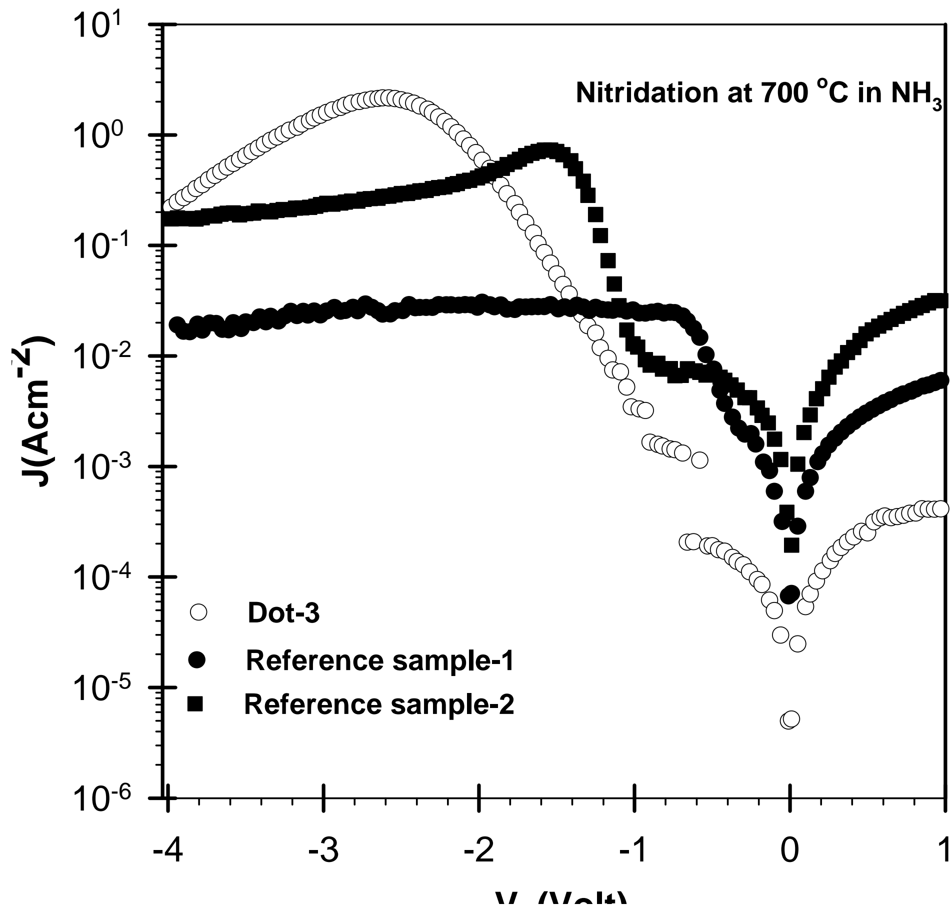


Figure 4.31. J-V characteristics of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 700ºC in NH_3 and that of the reference sample-1.

Complete understanding of the non ideal effects present in MOS capacitors requires calculation of theoretical capacitance-voltage characteristics. In Figure 4.32, $1/C^2$ versus gate voltage V_G curves are presented for four different MOS capacitors from the same substrate. All of the curves indicate identical slope resulting in a homogeneous acceptor concentration of $-2.5x10^{15}$ cm^{-3}. However, intercepts of the slopes on the V_G axis shows a large variation from -1.1 V to -2.1 V. It is inferred that density of effective oxide charges is not uniform in each sample. Using the experimentally derived parameters, theoretical C-V curves are calculated for each sample and presented together with experimental high frequency C-V curve. In Figure 4.33, theoretical and experimental C-V curves normalized to oxide capacitance are shown for Dot-3 together with conductance values of the same sample. A substantial shift of flat band voltage V_{FB} from the ideal C-V curve at V_G=0 V is almost equal to that found from Figure 4.32 within the experimental error. The value of V_{FB} seen in Figure 4.33 exists almost at the same V_G value of conductance peak as expected. However the extracted conductance values of the samples are higher than that of the samples nitrided in N_2O and reach the value of 500 μS which is very high for insulating properties. Using the V_{FB} voltage shift of each sample, effective oxide charge density, N_{eff}, of each sample were calculated using equation 3.29. The results of N_{eff} are given in Table 4.6. It is seen that the values of N_{eff} are almost similar to those found in nitrided samples in N_2O gas environment and much higher than the reference sample-1.

Finally the most important non ideal effect seen in MOS capacitors, the quality of Si-Ta_2O_5 interface was investigated. In Figure 4.34, surface potential ψ_s versus gate voltage V_G curves of four different MOS capacitors prepared after nitridation process in NH_3 at 700ºC are shown. Interface trap density D_{it} levels of samples were calculated using Terman's method and shown in Figure 4.35 together with those of reference samples. D_{it} levels are much lower than that of unnitrided reference sample-2 and closer to that of reference sample-1. D_{it} levels show variation around $(4\pm3)x10^{11}$ $(eVcm^2)^{-1}$, which are slightly higher than those found for MOS capacitors of nitridation in N_2O at 700ºC. It can be inferred that nitridation process in N_2O gas forms better interface between silicon and Ta_2O_5 oxide layer due to reach oxygen in N_2O.

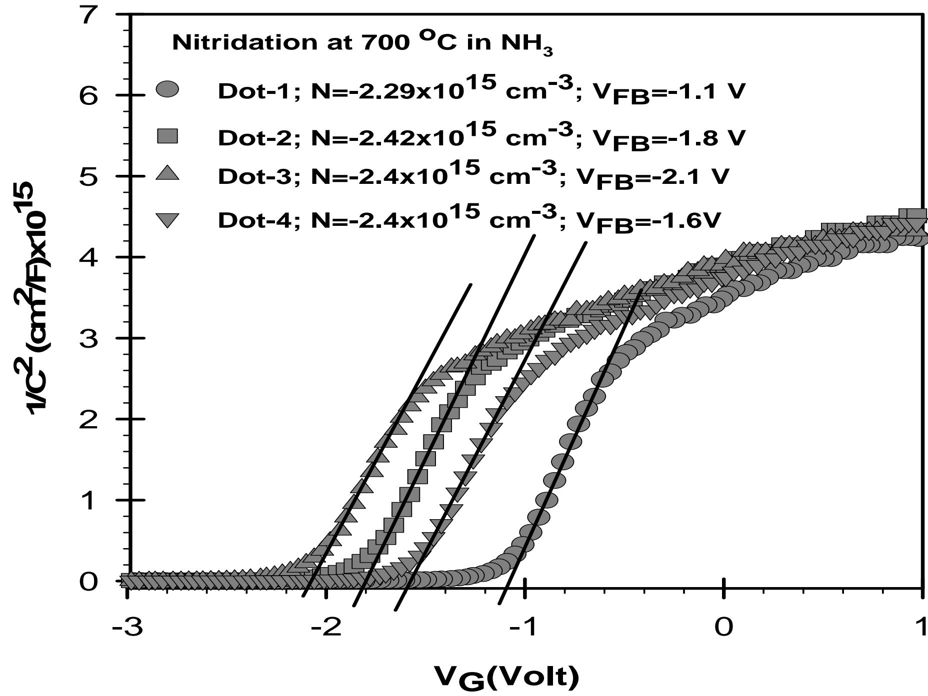


Figure 4.32. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation temperature at 700ºC in NH_3 gas environment

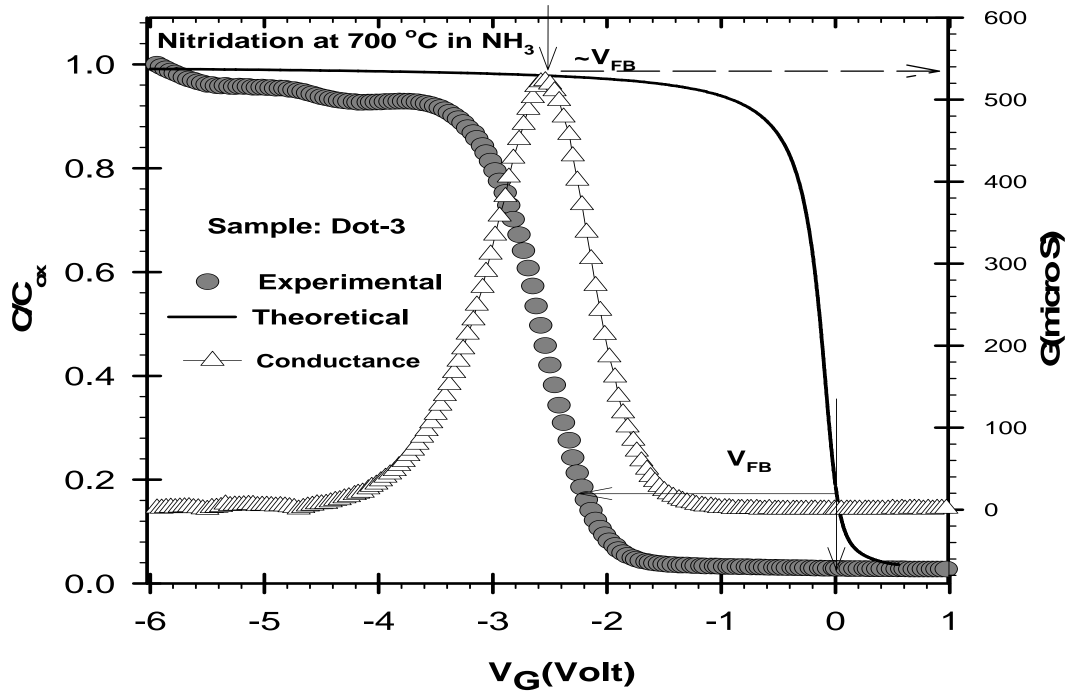


Figure 4.33. Conductance, G versus gate voltage and theoretical and experimental normalized high frequency capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 700ºC.

Table 4.6. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 700ºC in NH3 gas ambient

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} ($eVcm^2)^{-1}$
Dot-1	20	6.25 x10^{-4}	11.9	327	-2.3	-1.1	-1.2	6.2	29	6 ± 1
Dot-2			12.5	345	-2.4	-1.8	-2.1	6.2	51	4 ± 2
Dot-3			12.3	343	-2.4	-2.1	-2.3	6.2	61	4 ± 3
Dot-4			11.5	318	-2.4	-1.6	-1.7	6.7	38	5 ± 2

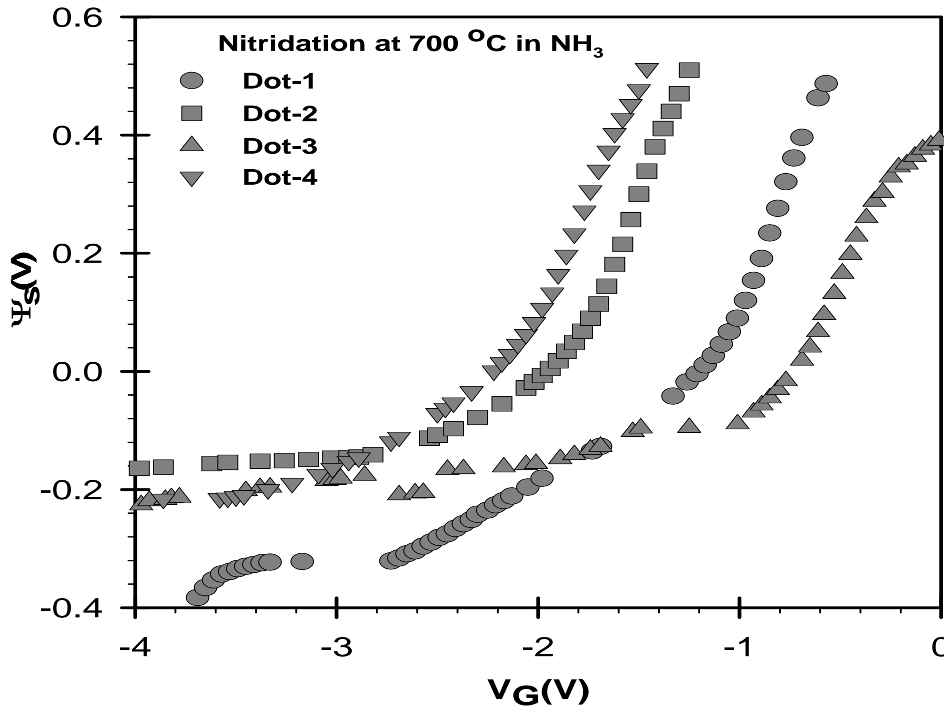


Figure 4.34. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox} curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 700ºC

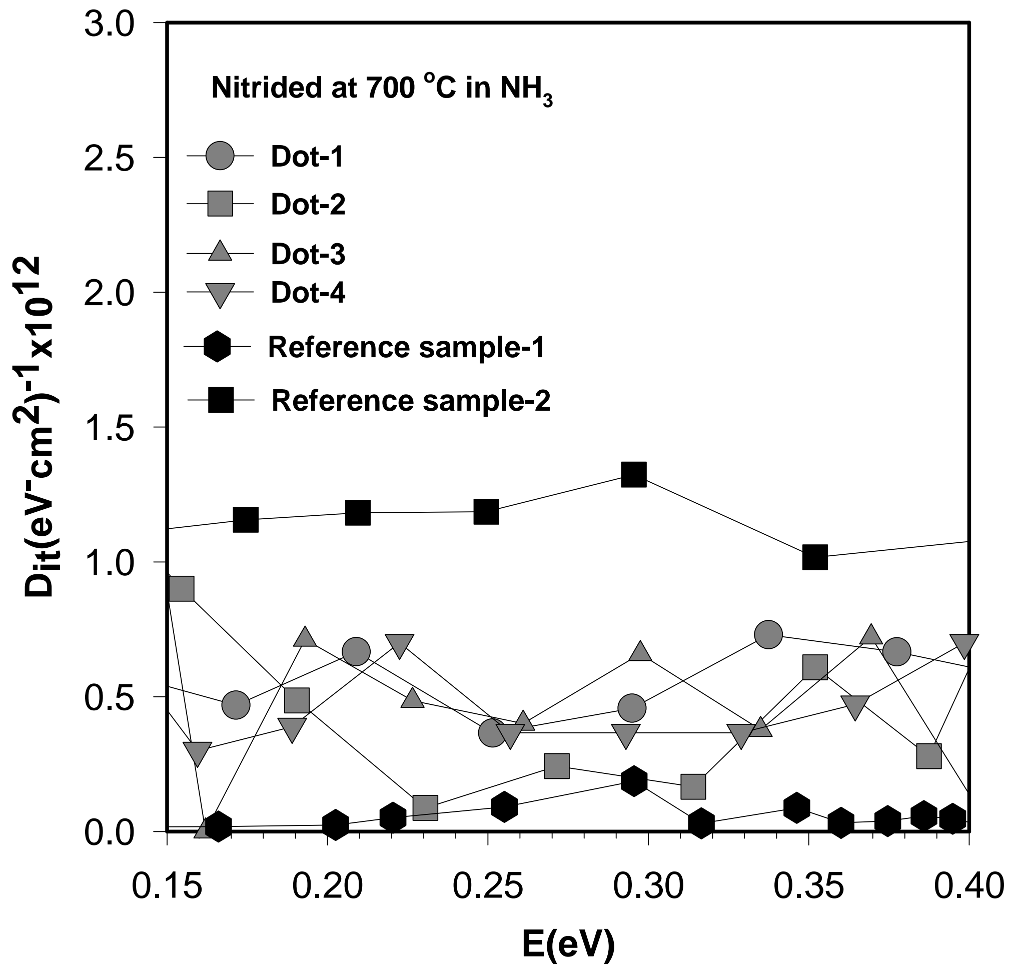


Figure 4.35. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 700ºC and for reference sample with native SiO_2

The last nitridation process was carried out at 800ºC in NH_3 gas. Experimental C-V curves of four different dots are shown in Figure 4.36. The oxide capacitance in accumulation region is 225 pF ± 5 pF for different dots. Dielectric constant derived from the oxide capacitance is around 8±0.4, which is lower than nitridation at 700ºC in the same gas ambient. The hysteresis effect on high frequency C-V curve of Dot-2 is presented in Figure 4.37. There is a counterclockwise behavior similarly obtained in other nitrided sample. The flat band voltage shift, ΔV_{FB}, is 800 mV indicating high level of mobile trap charges present in high-k Ta_2O_5 oxide layer. The positive mobile trap charge density corresponding to this voltage shift is equal to 1.8×10^{12} cm^{-2}. This is a serious non-ideal effect present in all high-k dielectrics and is necessary to be reduced to the level of native oxide SiO_2. On the other hand, leakage current characteristic of Dot-2 is shown in Figure 4.38. It is clearly seen that, the level of leakage current decreases to the level of reference sample-1 in inversion region. However, the leakage current density in depletion region at gate voltage around flat band voltage V_{FB} is almost two orders of magnitude higher than that of reference sample-1.

In order to investigate the effect of other non-ideal effect present in the Ta_2O_5 oxide layer and Ta_2O_5-Si interface, theoretical C-V characteristics are required to be calculated using the experimentally derived parameters. Doping concentration of p-type silicon substrate is calculated from the slope of $1/C^2$ versus V_G curves of the samples as shown in Figure 4.39. In addition, the intercept of the slope on V_G axis gives estimated flat-band voltage shift of C-V curves from the ideal C-V one. This is presented in Figure 4.40, where both experimental and theoretical capacitance values normalized to the oxide capacitance show a significant shift along the voltage axis V_G. It is clearly seen that there is a large flat band voltage shift indicating large density of effective oxide charge. For each sample, similar curves were calculated and reliable V_{FB} voltage shift were extracted. These flat band values are very close to those found from the intercept of the slope of $1/C^2$ vs V_G curves. In addition, the V_{FB} values were also confirmed by the peak position of conductance versus V_G, which exist around V_{FB} value on G versus V_G curve. In Figure 4.40, conductance versus V_G curve of the same sample is also shown, where peak position of G versus V_G is around V_{FB} voltage shift of experimental C-V curve. The obtained conductance values for these samples are in the same range as the previous sample.

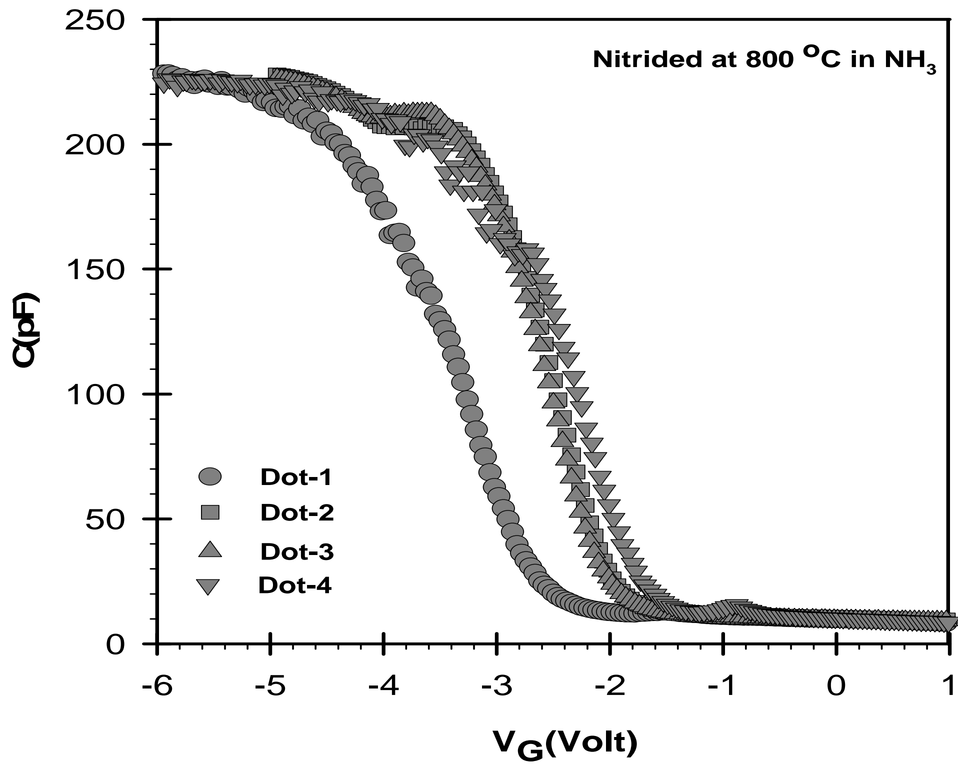


Figure 4.36. High frequency capacitance versus gate voltage curves of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 gas environment at 800ºC.

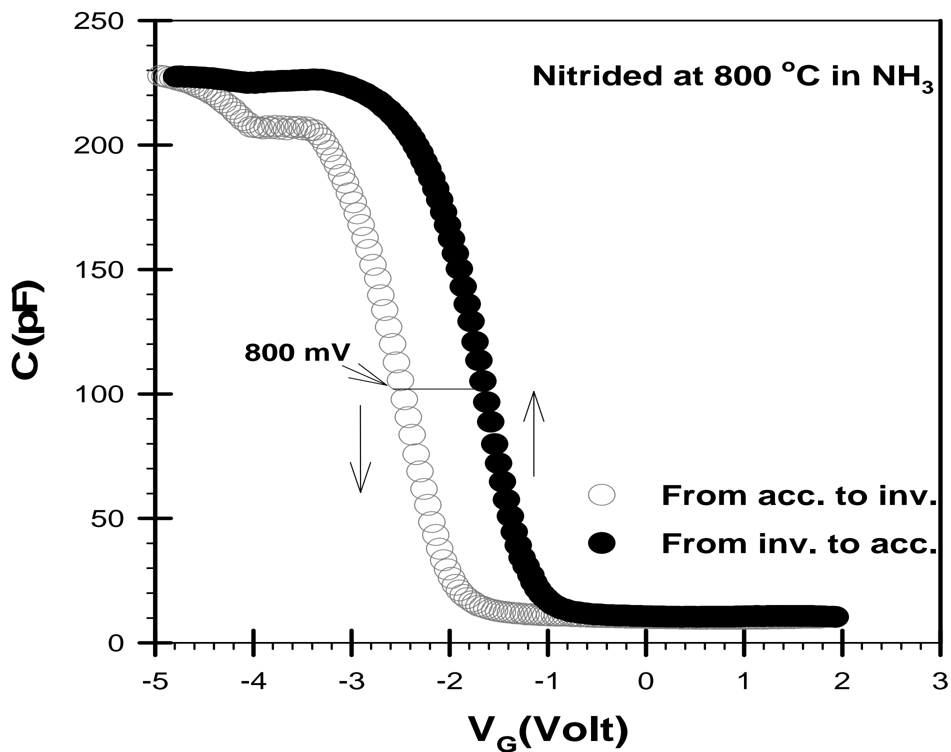


Figure 4.37. Forward and reverse C-V curve of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor with nitrided Si surface at 800ºC in NH_3

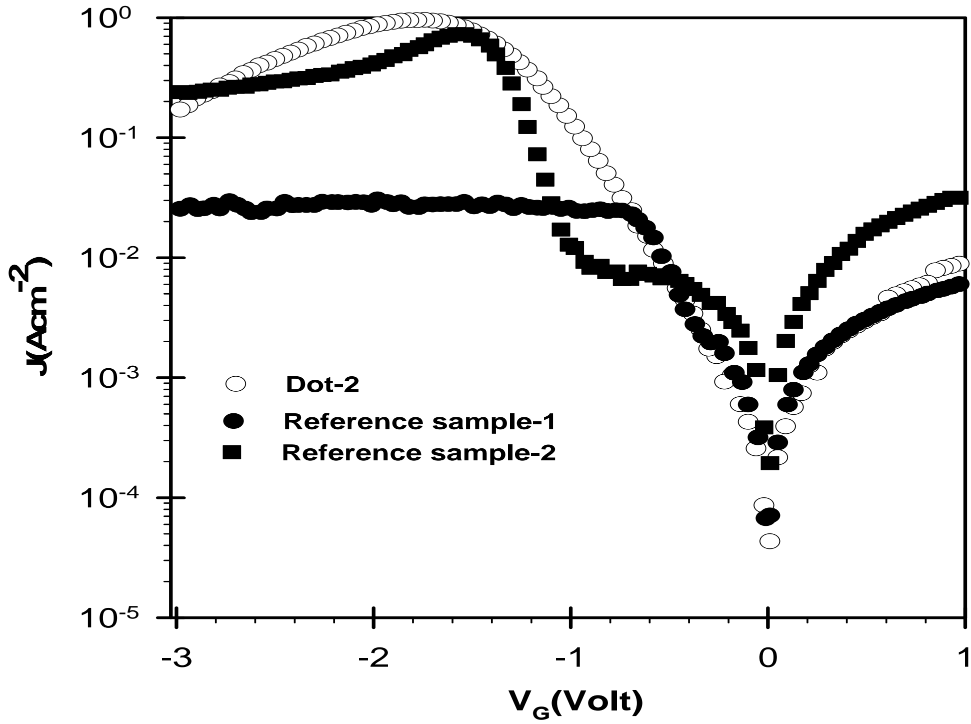


Figure 4.38. J-V characteristics of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 800ºC in NH_3 and that of the reference sample-1.

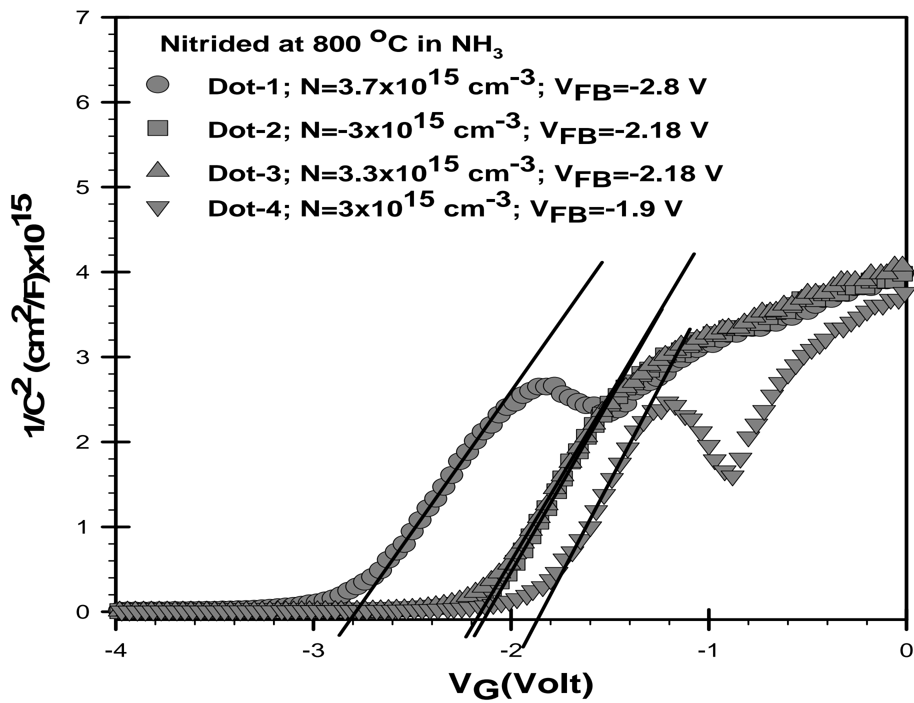


Figure 4.39. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation temperature at 800ºC in NH_3 gas environment

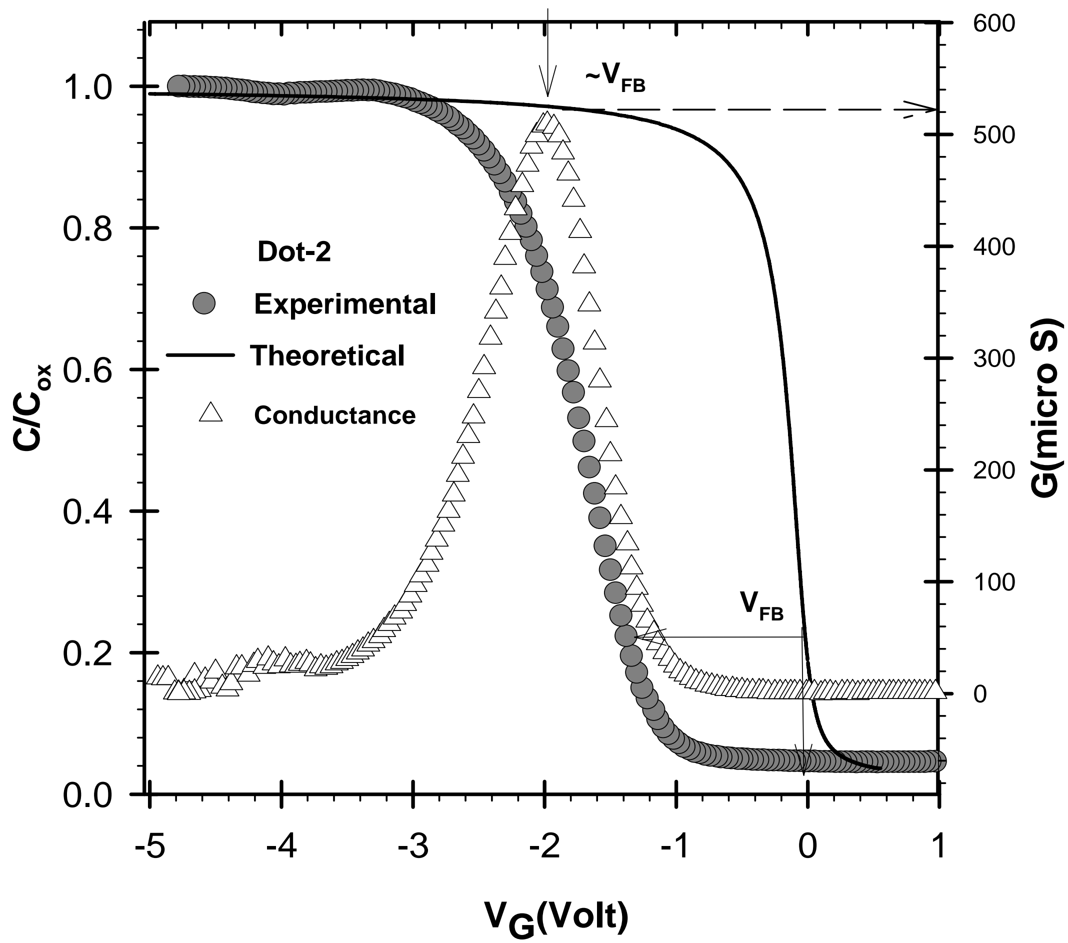


Figure 4.40. Conductance, G, versus gate voltage and theoretical and experimental normalized high frequency capacitance-voltage curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 800ºC.

The values of extracted V_{FB} are used to calculate the N_{eff} of each MOS capacitor taken from the same substrate. The V_{FB} values show a variation from -2,3 to -3.4 volt among the samples. Correspondingly, the calculated N_{eff} values show variation between $3.5x10^{12}$ cm^{-2} and $5.7x10^{12}$ cm^{-2} as summarized in Table 4.7. These levels are quite high for an oxide to be used in as a replacement of native oxide SiO_2.

Furthermore, the density of interface traps are calculated for the samples using ψ_s versus V_G curves shown in Figure 4.41 and procedure of Terman's Method. The resulting D_{it} levels of nitrided samples in NH_3 at 800 ^OC and that of reference samples are presented in Figure 4.42. The levels of D_{it} show a variation among the samples. It is around $5 \pm 3x10^{11}$ $(eVcm^2)^{-1}$, which is quite higher than that of reference sample-1. However it is substantially lower than that of unnitrided reference sample-2 with high-k dielectric. Additional research is required to improve the D_{it} level by improving Ta_2O_5-Si interface.

Table 4.7. Summary of parameter extracted from experimental high frequency C-V measurements of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 800ºC in NH_3 gas ambient.

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) $x10^{15}$	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} $x10^{11}$ (cm^{-2})	D_{it} $x10^{11}$ $(eVcm^2)^{-1}$
Dot-1	20	6.25 $x10^{-4}$	8.3	228	-3.6	-2.8	-3	9.4	57	7 ± 3
Dot-2			7.6	227	-3	-2.18	-2.3	9.4	42	6 ± 2
Dot-3			8.4	232	-3.3	-2.18	-2.3	9.5	42	4 ± 3
Dot-4			8.1	224	-3	-1.9	-2	9.6	35	5 ± 3

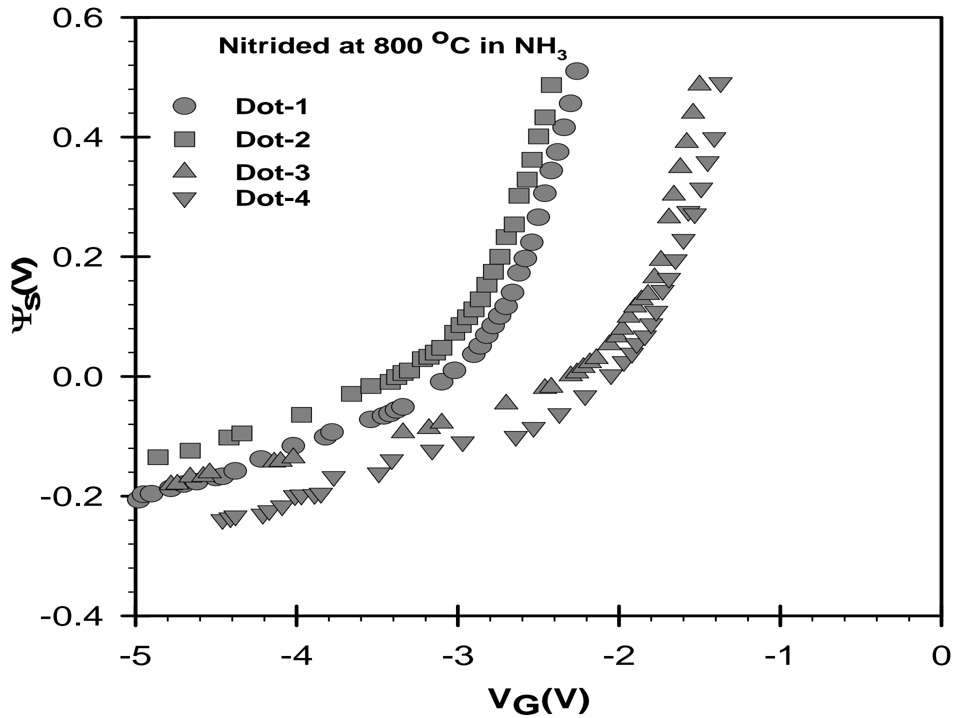


Figure 4.41. The surface potential ψ_s versus gate voltage V_G obtained from the normalized theoretical and experimental high frequency C/C_{ox}-V curves of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 800ºC

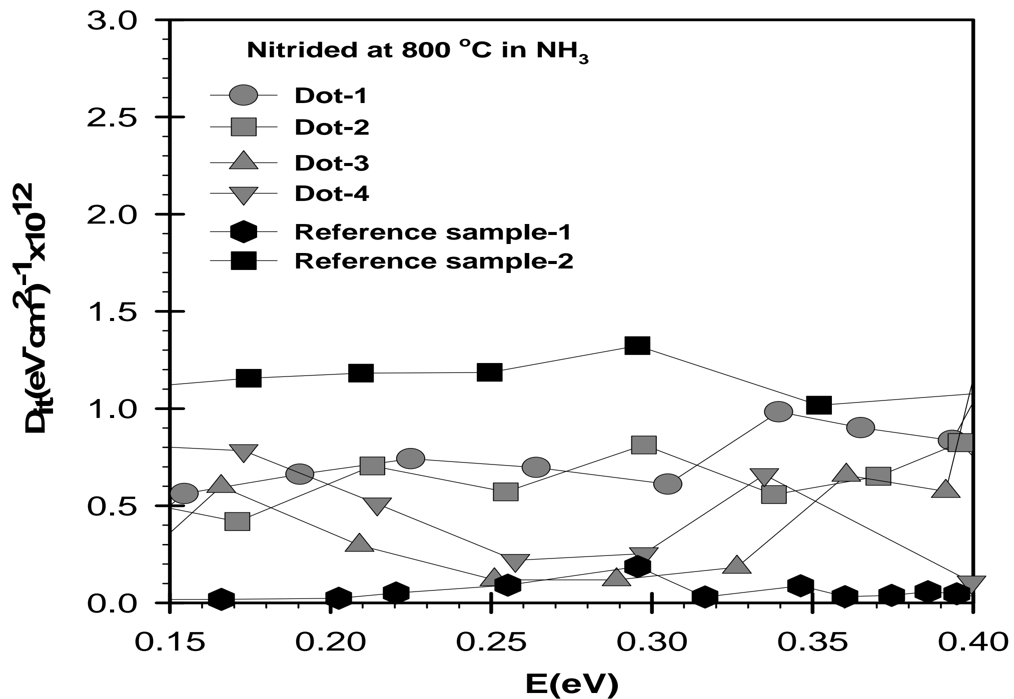


Figure 4.42. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in NH_3 at 800ºC and reference sample with native SiO_2

4.4.3 Conclusions

In this part of thesis, the first objective of thesis has been investigated using MOS capacitors with high-k Ta_2O_5 oxide layers and two reference samples. First group of samples was Al- (SiO_2)-Si MOS capacitor, as a reference sample-1. Second group of sample was Al-Ta_2O_5-(SiO_2)-Si MOS capacitor as reference sample-2. The last group of the samples was Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor, which was exposed to prior nitridation process in N_2O and NH_3 gas ambient before formation of oxide layers.

Analysis of high frequency C-V characteristics of Reference Sample 1 indicated that native oxide SiO_2 has the lowest moving trap charges with ΔV_{FB} less than 30 mV. The oxide capacitance for the predetermined gate area and oxide thickness resulted in the dielectric constant of 3.9 as found in the literature. The leakage current density in the depletion is around ~10^{-2} Acm^{-2} and conductance peak value was found to be 22 μS. The effective oxide charge density N_{eff} is around $2.9 x 10^{11}$ cm^{-2}, and the interface trap charge density is found to be $2 \pm 1 x 10^{11} (eVcm^2)^{-1}$. Both Terman's and simultaneous C-V method resulted in similar values.

In Reference Sample 2, replacement of SiO_2 with high-k Ta_2O_5 oxide layer increases the dielectric constant a factor of three. Due to thermal oxidation of Ta films on silicon (a smooth process), the level of moving trap charges is still as low as that observed in native oxide SiO_2. However, leakage current, effective oxide charges and density of interface trap states increase drastically. The peak values of conductance increased by several times and reach to the value of 90 μS and the leakage current reach to 1 Acm^{-2}. Due to such high leakage currents observed in high-k dielectrics, low frequency C-V measurement could not be carried out. Similarly, the effective oxide charge density increased to $3.2 x 10^{12}$ cm^{-2} which caused high flat band voltage shift in the experimental C-V curves. Interface quality between silicon and high-k Ta_2O_5 worsens and D_{it} level increases to the values of $1.1 \pm 2 x 10^{12}$ $(eVcm^2)^{-1}$.

In order to improve the interface quality of Si-Ta_2O_5, a novel approach known as prior nitridation of silicon surface before formation of Ta_2O_5 oxide layer was applied in N_2O and NH_3 gas ambients at different nitridation temperatures. For the samples nitrided in N_2O, the most promising dielectric constants and equivalent oxide thicknesses, which are around 10.2 and 7.5 nm, respectively, were obtained for the samples nitrided at 850 ^oC. Among the samples nitrided in NH_3, the best dielectric

constants and equivalent oxide thicknesses were obtained for the sample nitrided at 700 ^{o}C as 12 and 6.2 nm, respectively. In both nitridation processes, no improvement in leakage current levels was observed. Both the conductance and effective oxide charge density increased several times. On the other hand, among the nitrided samples, nitridation in N_2O provide lower conductance and effective oxide charge values which are around 350 μS and 30-50x10^{11} cm^{-2}, respectively. For the samples nitrided in NH_3 these characteristics were obtained as 500-600 μS and 30-60x10^{11} cm^{-2}, respectively. The most important benefit of the nitridation process is the improvement in density of interface trap states. For the samples nitrided in N_2O, D_{it} level decreased to the level of Reference Sample 1 with native oxide SiO_2. It decreases from 1.1±2x10^{12} $(eVcm^2)^{-1}$ to the levels of 3±1x10^{11} $(eVcm^2)^{-1}$. For the case of NH_3 nitridation, the levels of D_{it} improves from the unnitrided Reference Sample 2, however, slightly higher values were obtained as compared to N_2O nitrided samples.

4.5 The Effects of Metal Gates in MOS Characteristics

A wide variety of metal gates are currently being evaluated as replacements for n+ and p+ poly silicon gate on high dielectric constant gate dielectrics in CMOS circuit since they would eliminate the problems of dopant penetration and poly-silicon depletion currently seen in poly-Si gates due to their high carrier density. Therefore, understanding the metal gate electrode - gate dielectric interface is critical in device performance. In this study, the effect of three metal gate electrodes has been investigated in contact with Ta_2O_5 gate dielectric. In this part of thesis, four groups of samples are used. First group has the structure of Al metal gate- $Ta_2O_5(SiO_2)$-Si MOS capacitor, where Ta_2O_5 oxide layer is formed by thermal evaporation of reactively sputtered Ta films on silicon substrate. Second group of sample have the structure of Al metal gate-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor, where a prior nitridation of silicon surface in N_2O has been carried out before Ta_2O_5 oxide formation. Oxide layer is deposited using RF sputtering from Ta target in Ar and O_2 gas. Finally Al metal gates were evaporated on Ta_2O_5 oxide layer. The third group of samples has the form of TiN metal gate-$Ta_2O_5(SiO_2)$-Si MOS capacitor. Here, Ta_2O_5 oxide layer is formed using thermal oxidation of reactively sputtered Ta metal films on silicon surface and TiN

metal gate was deposited using RF magnetron sputtering on Ta_2O_5 oxide layer. The fourth group of samples has W metal gate and has the structure of W metal gate-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor. In this group, a prior nitridation of Si surface in N_2O at 700 ^oC and 850 ^oC using RTN process was applied before Ta_2O_5 formation. Oxide layer was deposited using RF magnetron sputtering from Ta target in Ar and O_2 gas mixture. High frequency C-V spectroscopy has been used to obtain the C-V characteristics of the samples. Important device parameters such as doping concentration, flat band voltage, dielectric constant, effective oxide charge and density of interface trap states were derived and the results were compared with the results of the Al-SiO_2-Si MOS capacitors, reference sample-1.

4.5.1 Results of Al Metal Gate MOS Capacitor

In this section, Al metal gate was used in two different groups of samples; the first one is the reference sample-2 and the second group is the nitrided samples in N_2O at 700 ^oC and 850 ^oC. The results of these two groups of samples were already presented at the beginning of their chapter. However, they will be summarized in this part of thesis in order to compare these results with those of other MOS capacitors having gate metal of TiN and W.

In Figure 4.43, example of high frequency C-V curves of MOS capacitors with aluminum gate metal are presented for each sample. The results of only one characteristics dot from each substrate was taken for the representation. Main differences among the Al gate metal of these MOS capacitors are the effect of prior surface nitridation process of silicon surface. It is seen that the oxide capacitance and corresponding dielectric constant is the highest for Al-Ta_2O_5(SiO_2)-Si unnitrided capacitor. Thermal oxidation of Ta_2O_5 gives better quality oxide layer. In addition, hysteresis behavior of the Al metal gate samples are summarized in Figure 4.44, where Al-Ta_2O_5(SiO_2)-Si unnitrided sample shows almost insignificant ΔV_{FB} voltage shift in hysteresis of high frequency C-V curve. However, other Al-Ta_2O_5-SiO_xN_y-Si MOS capacitors with a prior nitridation of silicon surface indicate higher ΔV_{FB} voltage shifts up to 800 mV among different dots taken from the substrate. It can be concluded that the mobile trap charges are almost insignificant in thermally grown Ta_2O_5 of reference

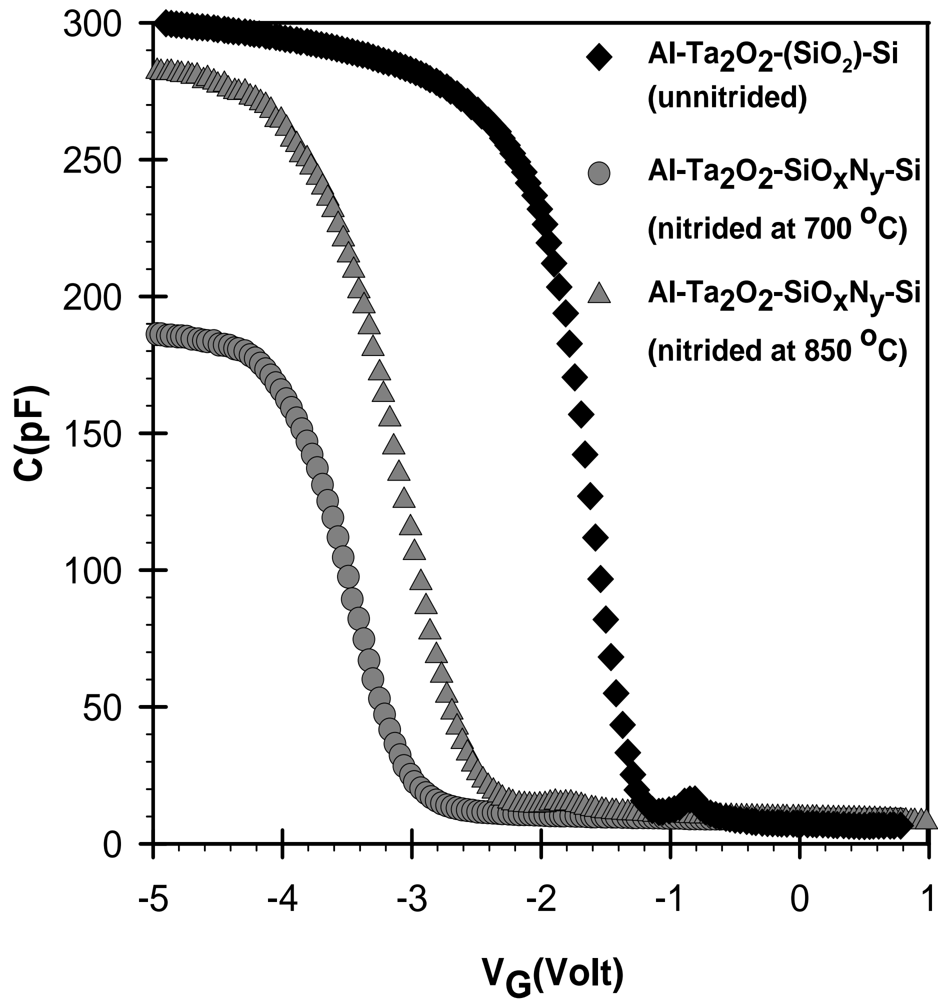


Figure 4.43. High frequency capacitance versus gate voltage curves of MOS capacitor with Al metal gates

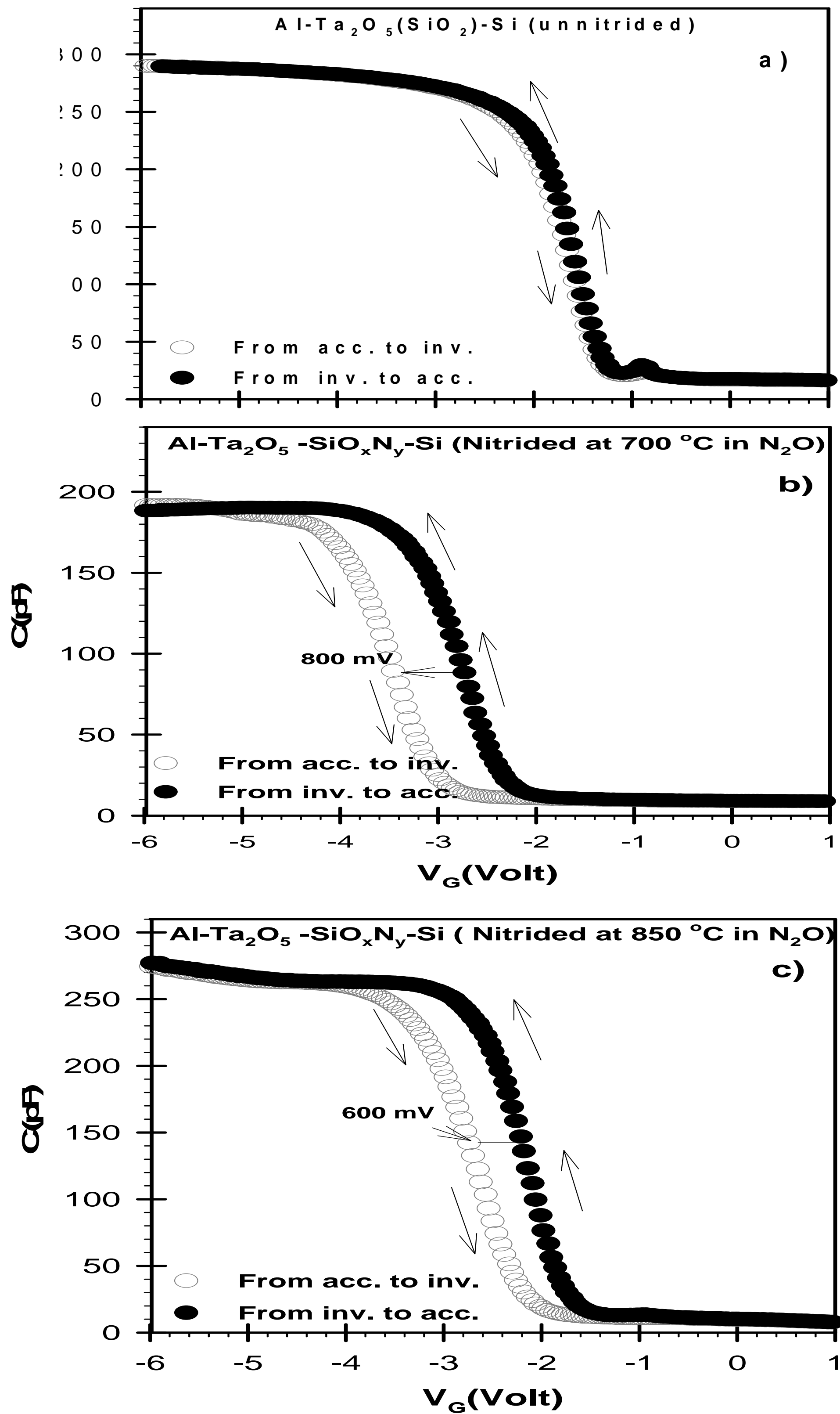


Figure 4. 44. Hysteresis behavior of high frequency C-V curve of a) Al-Ta_2O_5(SiO_2)-Si reference sample-2, b) Al-Ta_2O_5-SiO_xN_y-Si (nitrided sample at 700ºC), c) Al-Ta_2O_5-SiO_xN_y-Si (nitrided sample at 850ºC) MOS capacitors

sample-2, however their density is substantially higher for Ta_2O_5 oxide layers prepared with RF magnetron sputtering on the nitrided silicon surface in N_2O gas. The leakage currents of Al metal gate MOS capacitor are summarized in Figure 4.45. Even though lower leakage currents are measured in inversion region of MOS capacitors, much higher leakage currents are obtained in depletion region for reference sample-2 and nitrided samples in N_2O than that of reference sample-1 with Al-SiO_2-Si structure. Such high level of leakage currents are unavoidable feature of high-k oxide layers independent of processing method used in MOS processing.

Finally, the interface quality of Ta_2O_5-Si structure is summarized in Figure 4.46 for Al metal gate samples. D_{it} level is high for thermally grown Ta_2O_5 on silicon surface, where not well defined interface with defects occurs. However, D_{it} levels of Al-Ta_2O_5-SiO_xN_y-Si MOS capacitors prepared after nitridation process of silicon surface in N_2O gas at 700 ^oC and 850 ^oC are very close to the level of Al-SiO_2-Si reference smple-1. It is inferred that prior nitridation process of silicon surface before oxide formation is a promising method to improve the interface quality of Ta_2O_5-Si structure.

Furthermore, summary of results obtained from the analysis of high frequency C-V curve of Al metal gate MOS capacitors are presented in Figure 4.8. Even though there is in D_{it} levels, the effective oxide charges are substantially high in all MOS capacitors with Ta_2O_5 oxide layers. The N_{eff} values are one order of magnitude higher than that of reference sample-1. But the lowest density of mobile trap charges is present in thermally grown Ta_2O_5 layers in reference sample-2.

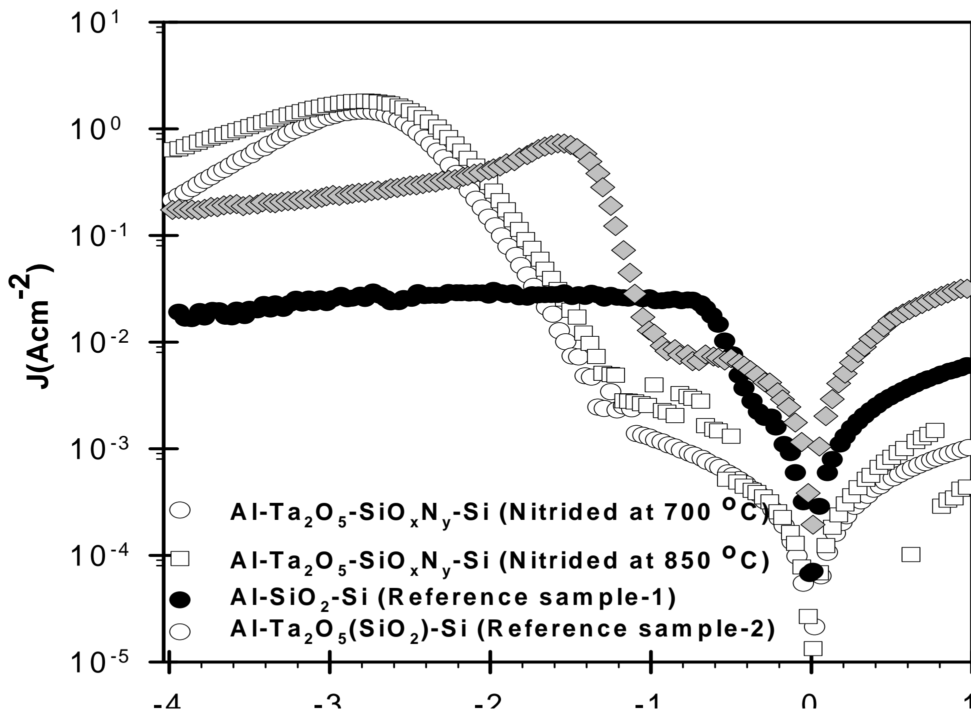


Figure 4.45. J-V characteristics of unnitrided reference sample-2, reference sample-1 and samples prepared after nitridation process at 700 and 850ºC in N_2O

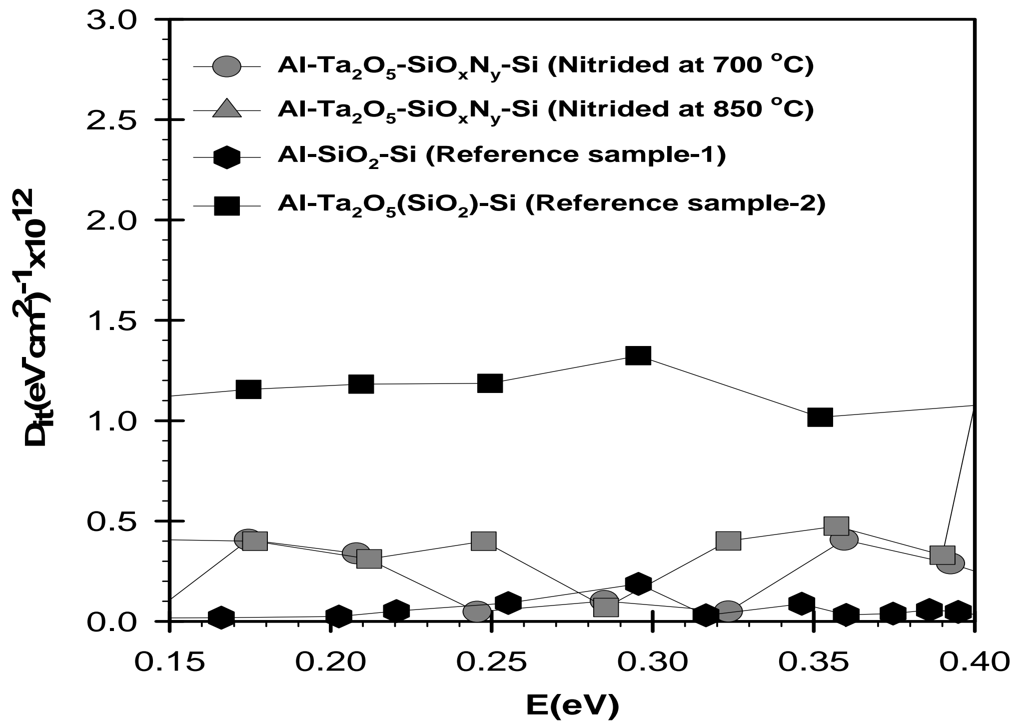


Figure 4.46. Density of interface states as a function of energy in the band gap of crystalline silicon for reference sample-1, unnitrided reference sample-2 and samples prepared after nitridation process at 700 and 850ºC in N_2O

Table 4.8 Summary of parameter extracted from experimental high frequency C-V measurements of Reference sample-1, Reference sample-2 and nitrided Al-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process at 700ºC and 850 ºC in N_2O gas ambient

Sample	t_{ox} (nm)	S (cm2)	k	C_{ox} (pF)	Na (cm^{-3}) $x10^{15}$	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} $x10^{11}$ (cm^{-2})	D_{it} $x10^{11}$ ($eVcm^2)^{-1}$
Ref. 1	20	1.96 $x10^{-3}$	3.9	345	-0.9	-0.6	-0.6	----	2.9	2±1
Ref.-2		6.25 $x10^{-4}$	11.2	310	-1.3	-1.35	-1.4	6.9	32	10±2
Nitrided at 700 °C		6.25 $x10^{-4}$	6.9	190	-2.4	-3.2	-3.3	11.4	30-50	3 ± 1
Nitrided at 850 °C		6.25 $x10^{-4}$	10.2	285	-2.4	-2.3	-2.5	7.5	30-50	4 ± 1

4.5.2 Results of TiN Metal Gates MOS Capacitor

In order to compare the effects of different metal gates formed on Ta_2O_5 high-k oxide layers, TiN metal contacts are deposited on thermally grown Ta_2O_5 layer using RF magnetron sputtering method. In this group of samples, Ta_2O_5 oxide layer was prepared using dry oxidation of Ta thin films deposited on silicon surface without any nitridation process similar to the reference sample-2 with Al metal gate. After TiN deposition, sample was exposed to H_2 annealing process in order to remove the oxide charges from the MOS capacitors. The reason of why TiN metal gate is that it is an important reinforcement candidate material as it has high hardness, stability at high temperature, excellent corrosion resistance and higher melting point than Al with 4.95 eV work function difference.

The high frequency C-V curves of four different dot of TiN-Ta_2O_5(SiO_2)-Si MOS capacitors taken from the same substrate are shown in Figure 4.47.Oxide capacitance with TiN metal gate is around 230 pF, which are lower than reference sample-2 with same oxide layer and Al metal gate. The dielectric constant calculated using this oxide capacitance and precisely measured oxide thickness is 6.6±0.02 among

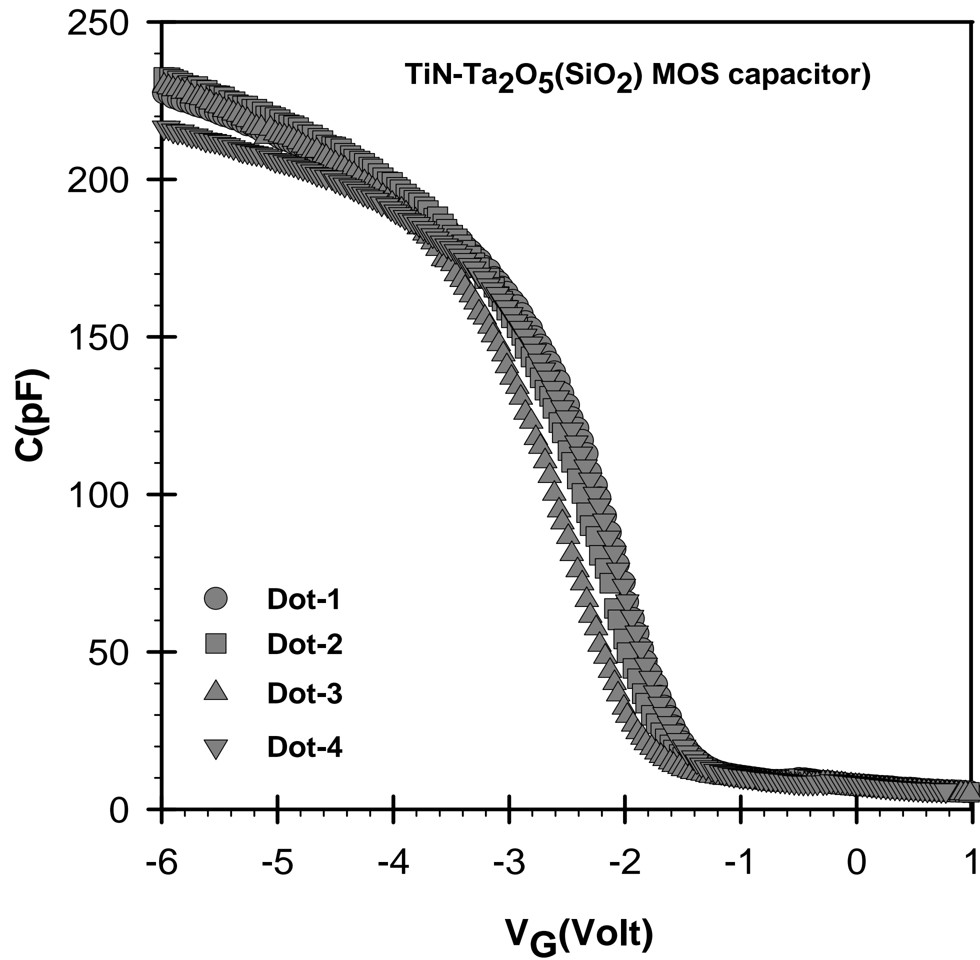


Figure 4.47. High frequency capacitance versus gate voltage curves of and four different dots of TiN-Ta_2O_5-(SiO_2)-Si MOS capacitor

different dots. This is one of the major differences from Al metal gate MOS capacitor with the same quality Ta_2O_5 oxide layer. The reduction in the effective dielectric constant could be due to a formation of interfacial layer between TiN metal gate and Ta_2O_5 oxide at top interface with lower dielectric constant. In addition, there is a slight variation in oxide capacitance among the dots as shown in Figure 4.47. It causes a variation in the electrical thickness of approximately 2 nm among the dots.

Doping concentration of silicon substrate and flat band voltage shift of experimental C-V curves are obtained from the $1/C^2$ versus V_G curves presented in Figure 4.48. N_A is found to be $3.0\pm0.5\text{x}10^{15}$ cm^{-3} and V_{FB} values change between 1.60 V and 2.05 V among the samples.

The effect of mobile trap charges present in TiN-Ta_2O_5(SiO_2)-Si MOS capacitors is shown in Figure 4.49, where the hysteresis behavior of high frequency C-V measurement indicate insignificant ΔV_{FB} voltage shift the same as found in reference sample-2 with Al metal gate and same quality Ta_2O_5 oxide layer grown by dry oxidation process. It can be concluded that thermal oxidation of Ta metal films deposited on silicon surface without any nitridation process results in Ta_2O_5 oxide layer with the lowest density of mobile trap charges present in the oxide charges. Since there is no damage in Ta_2O_5 oxide layer during oxidation in contrast to the RF magnetron sputtering of Ta_2O_5 oxide layers in Ar and O_2 gas environment. Furthermore, the leakage current density of Dot-3 shown in Figure 4.47 is shown together with reference samples in Figure 4.50. In inversion region, slightly lower leakage currents are measured than that of reference sample-1 with native oxide SiO_2, however, in more important part of gate voltage V_G, depletion region of devices both Al metal gate and TiN metal gate MOS capacitors with the same quality Ta_2O_5 oxide exhibit much higher leakage currents than reference sample-1. This is the main drawback of high-k oxide layers.

Ideal C-V curves of TiN metal gate samples were calculated using the parameters obtained from high frequency C-V curves and plotted together with the experimental C-V curves. It was found that similar V_{FB} voltage shifts exist as found from $1/C^2$ versus V_G plots. By using both theoretical and experimental C-V curves

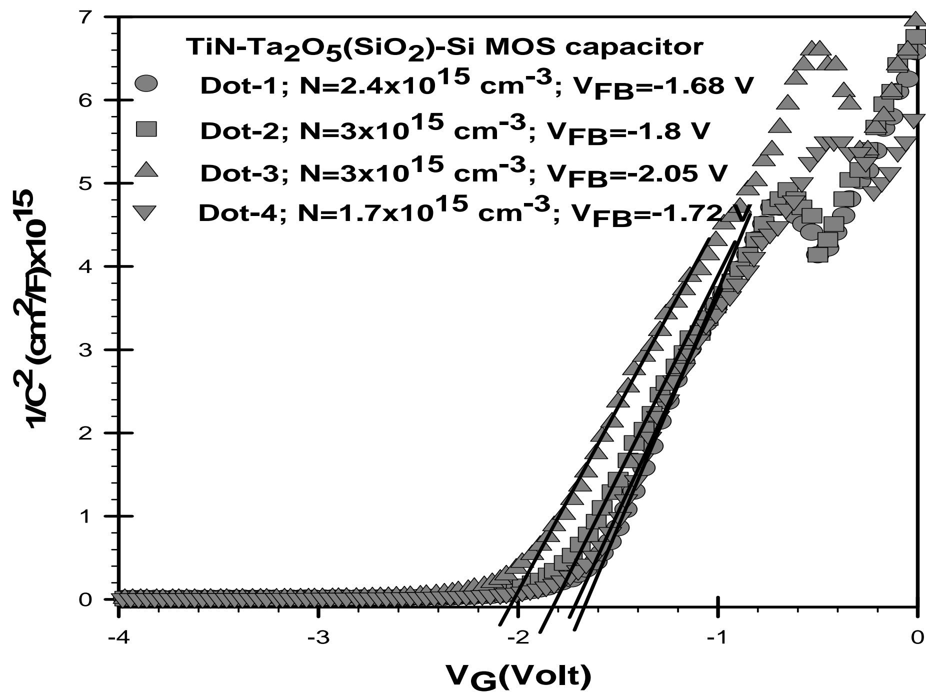


Figure 4.48. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of TiN-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor

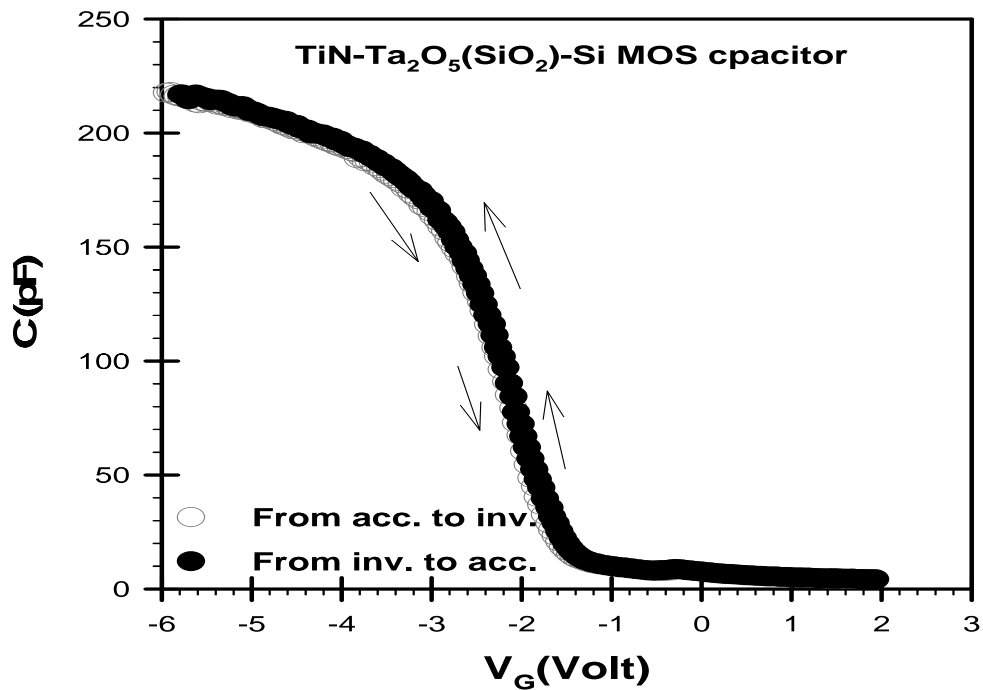


Figure 4.49. Forward and reverse C-V curve of TiN-Ta_2O_5-(SiO_2)-Si MOS capacitor with un-nitrided Si surface

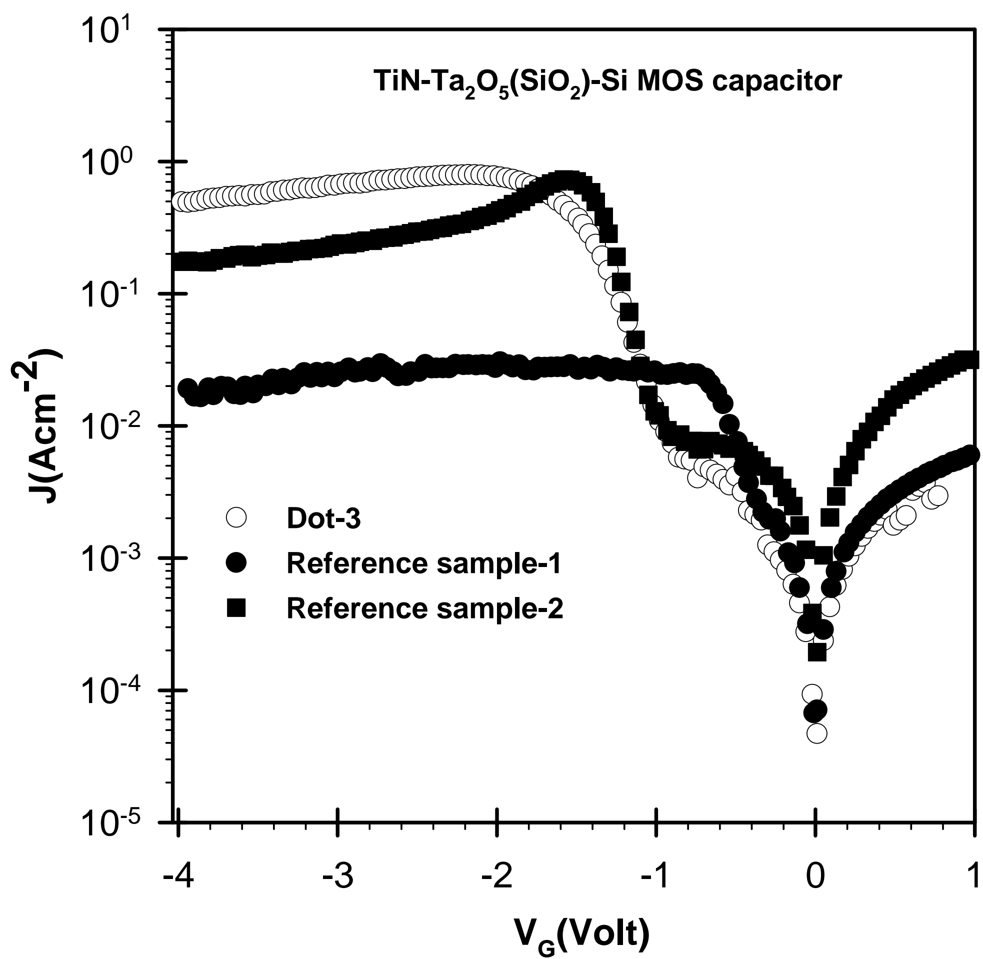


Figure 4.50. J-V characteristics of TiN-Ta_2O_5-(SiO_2)-Si MOS capacitor

normalized to the oxide capacitance, surface potential ψ_s versus gate voltage V_G curves were generated similarly carried out for previous samples (data not shown). Finally, D_{it} levels of TiN metal gate samples were calculated as a function of energy and shown in Figure 4.51. D_{it} levels are slightly lower than reference sample-2 with Al metal gate. However, there is a large variation D_{it} between $1x10^{11}$ $(eVcm^2)^{-1}$ and $8x10^{11}$ $(eVcm^2)^{-1}$. It can be inferred that interface of Ta_2O_5 and silicon substrate is irregularly modified to give slightly lower D_{it} values than that of Al metal gate sample. The important data obtained from high frequency C-V measurement for TiN-Ta_2O_5(SiO_2)-Si MOS capacitors is summarized in Table 4.9.

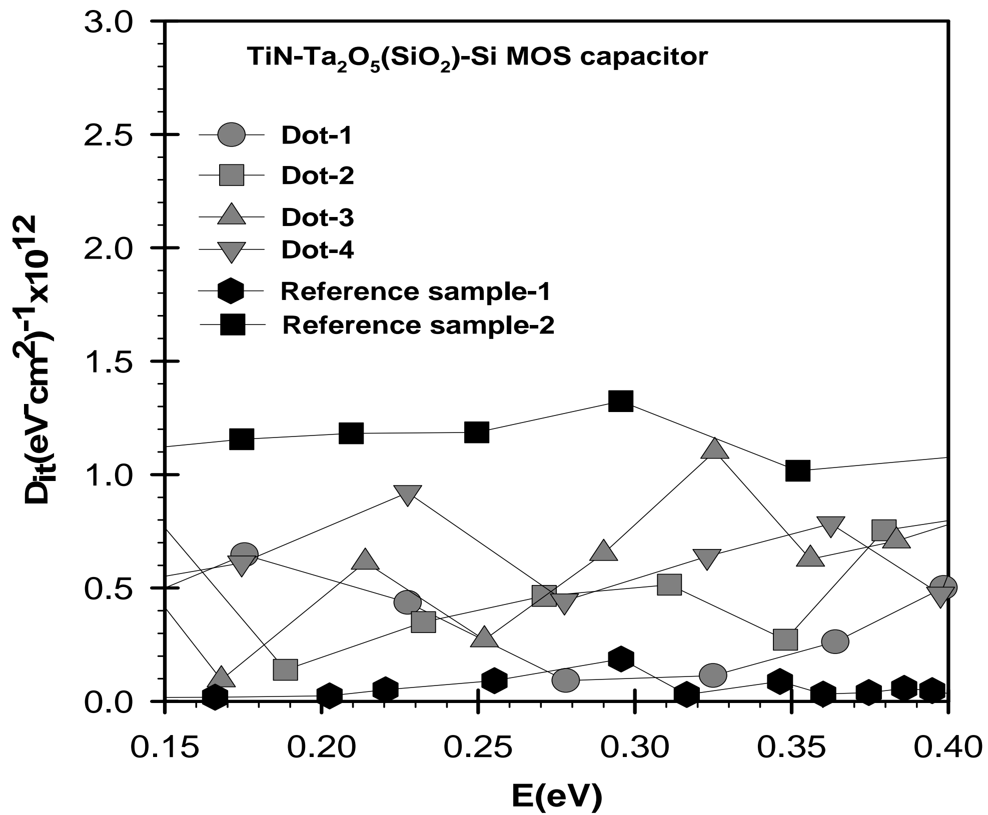


Figure 4.51. Density of interface states as a function of energy in the band gap of crystalline silicon for four different dots of TiN-Ta_2O_5-(SiO_2)-Si MOS capacitor and reference sample with native SiO_2

Table 4.9. Summary of parameter extracted from experimental high frequency C-V measurements of TiN-Ta_2O_5-Si MOS capacitor

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} ($eVcm^2$)$^{-1}$
Dot-1	15	6.25 x10^{-4}	6.4	236	-2.4	-1.68	-1.7	9.1	52	4±2
Dot-2			6.6	244	-3	-1.8	-1.9	8.8	57	3±2
Dot-3			6.6	245	-3	-2.05	-2	8.7	63	7±4
Dot-4			6.1	223	-2.6	-1.72	-1.7	9.6	50	6±3

4.5.3 Results of W Metal Gate MOS Capacitor

An alternative gate material is selected as tungsten. It is a steel-gray to tin-white metal with the highest melting of all metals. It has the highest tensile strength and excellent corrosion resistance. It shows no inter diffusion with the surrounding materials and smooth interface with dielectrics. Its work function is 4.5 eV. The fifth group of samples used in this thesis was prepared using W metal gate. In this group of samples, RTN process of silicon surface at 700 ^oC and 850 ^oC in N_2O was applied. Then the Ta metal films were deposited by RF sputtering method. Dry oxidation of Ta film in O_2 at 873 ^oC was carried out to form high-k Ta_2O_5 oxide layer. Finally, W metal gate electrodes were deposited on the oxide using RF sputtering method.

High frequency C-V measurements of several dots from the same substrate were shown in Figure 4.52a for nitrided sample at 700 ^oC and in Figure 4.52b for nitrided sample at 850 ^oC. The oxide capacitance for both samples is around 300±15 pF, it shows slight changes among different dots. Dielectric constant calculated from these oxide charges is 12±0.5 and the equivalent oxide thickness for all dots in both groups of samples is 7±0.2 nm, giving consistent value among different dots. It can be understood that nitridation in N_2O at 700 ^oC and 850 ^oC give almost identical quality oxide layer.

High frequency C-V curves of the samples are used to generate $1/C^2$ versus gate voltage V_G in order to obtain doping concentration N_A and flat band voltage shifts due to non ideal effects. In Figure 4.53, $1/C^2$ vs V_G plots of W metal gate MOS capacitors are presented. The value of N_A is found to be $2.5x10^{15}$ cm^{-3} for 700 ^oC samples and $5x10^{15}$ cm^{-3} for 850 ^oC samples. Both groups of samples show substantial flat band V_{FB} voltage shifts around -2 V.

The effect of mobile trap charges were characterized by measuring hysteresis behavior of high frequency C-V curves from accumulation to inversion and back to accumulation. Examples of hysteresis measurement of one of the Dot from each group of samples are presented in Figure 4.54a and Figure 4.54b, for 700 ^oC and 850 ^oC samples, respectively. It is important to note that ΔV_{FB} voltage shift in hysteresis curve is almost insignificant to notice. It is below 30mV and in the acceptable limit of electronic fabrication of MOS devices. Such low mobile trap charges were measured in MOS capacitors with thermally grown Ta_2O_5 oxide layers. These samples are the reference sample-1 with Al metal gate and the group for sample with TiN metal gate. It

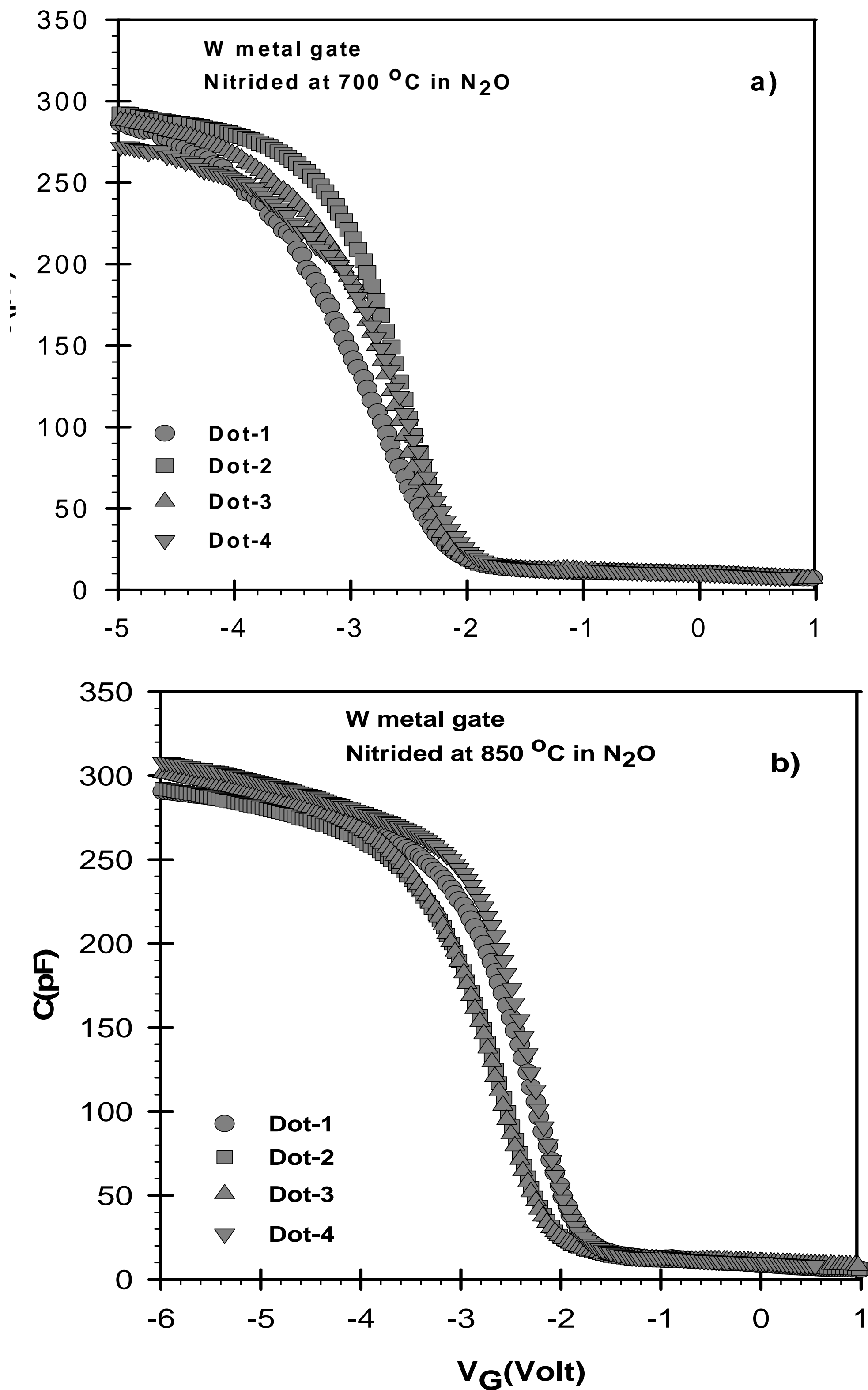
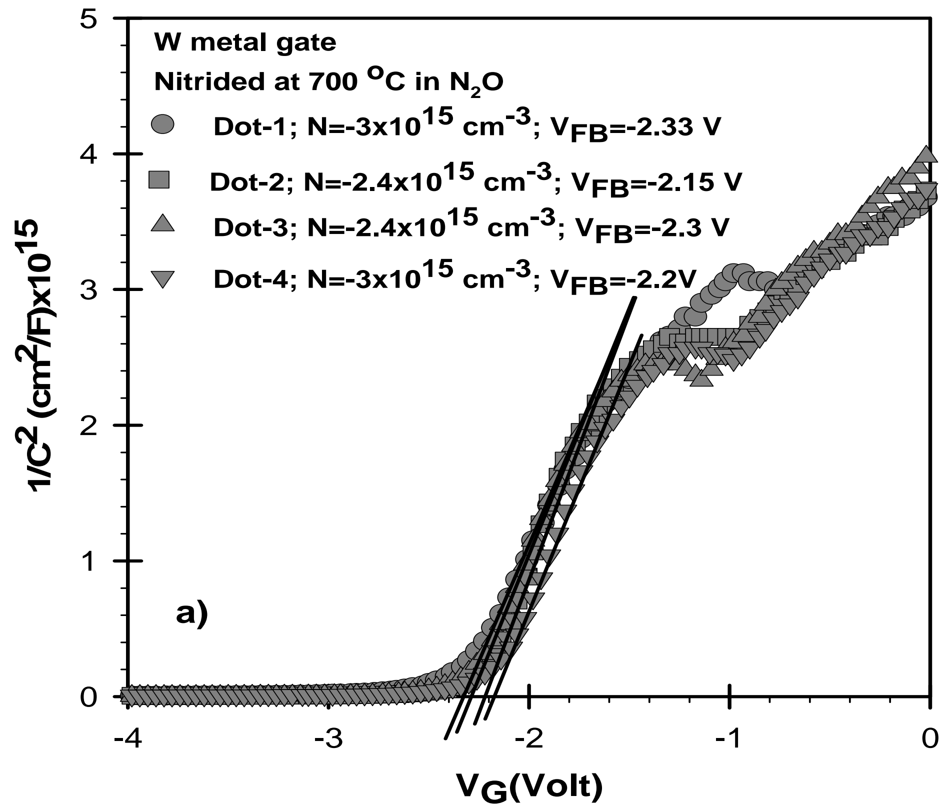


Figure 4.52. High frequency capacitance versus gate voltage curves of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitors for nitridation temperatures at a) 700ºC, b) 850ºC in N_2O gas environment



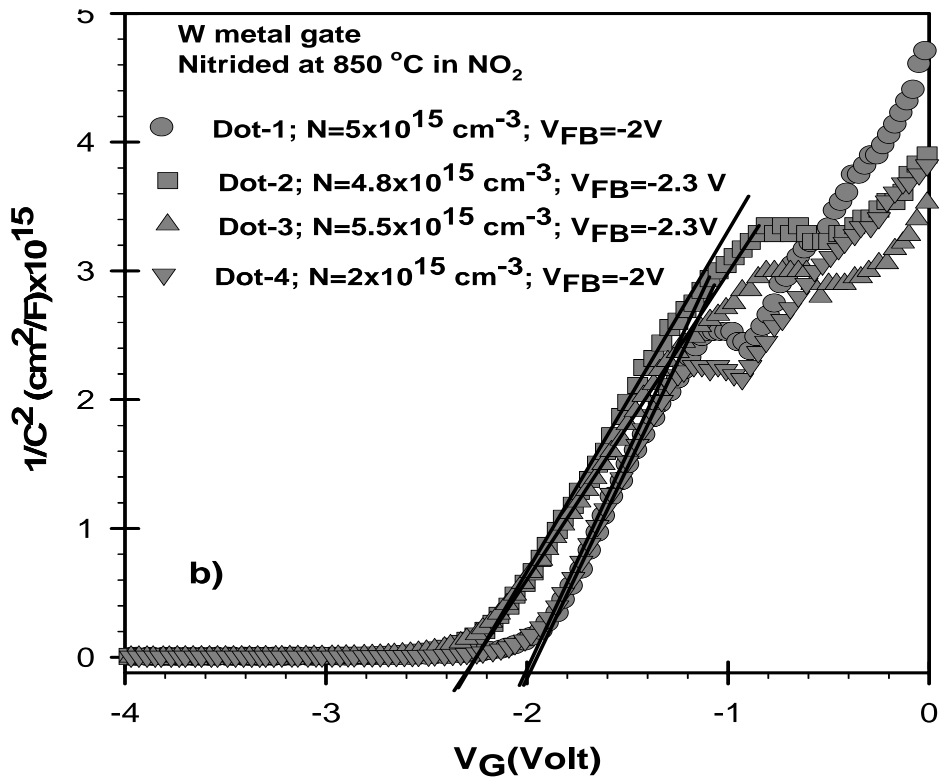
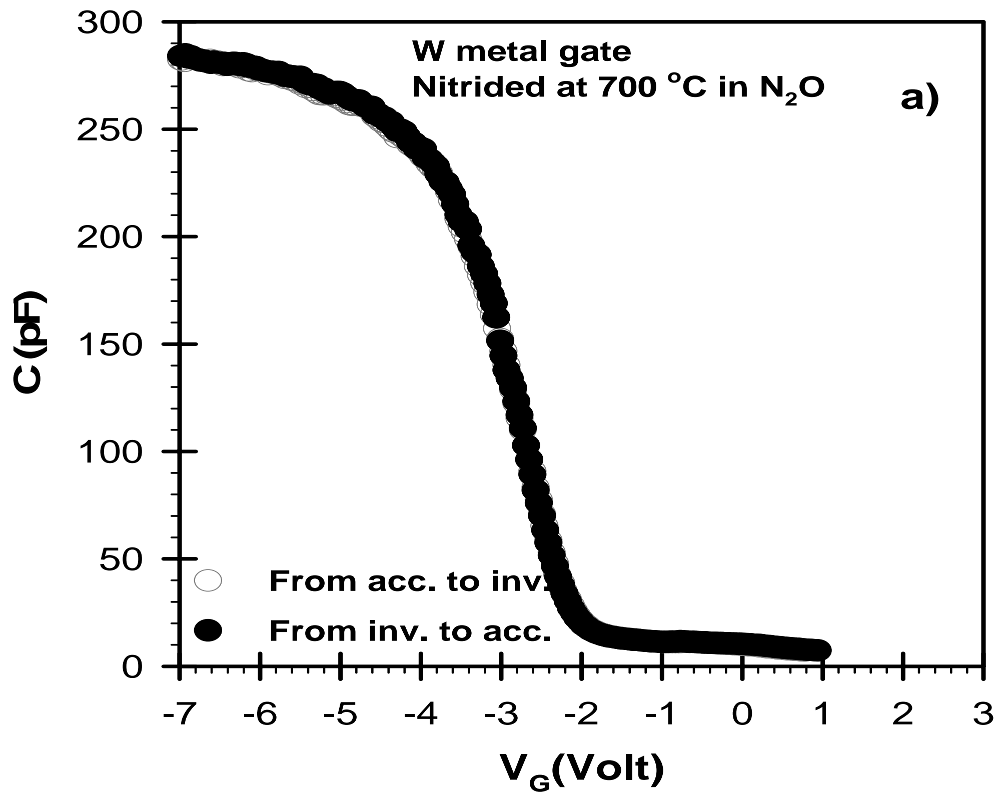


Figure 4.53. Experimental $1/C^2$ versus gate voltage V_G graph of four different dots of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation in N_2O gas environment at a) 700 ºC, b) 850 º



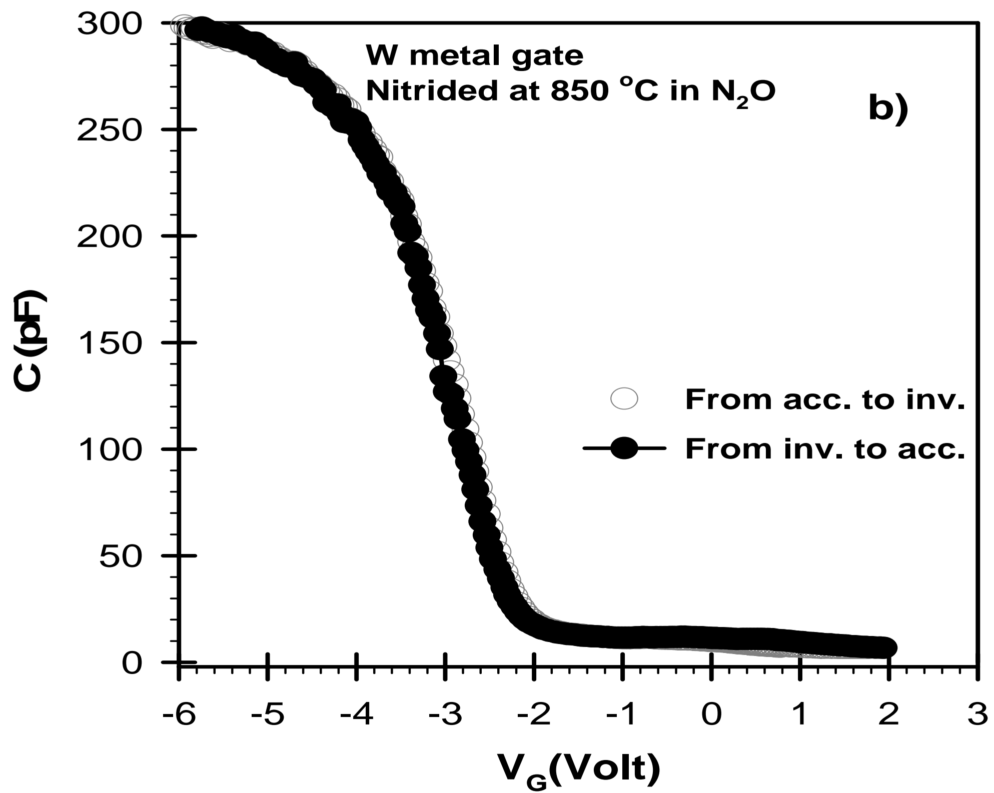


Figure 4.54. Forward and reverse C-V curve of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor with nitrided Si surface in N_2O at a) 700ºC, b) 850ºC

can be concluded that thermal oxidation of Ta metal films contain almost insignificant mobile trap charges in contrast to those deposited by RF sputtering process.

Leakage current measurement of W metal gate samples are shown in Figure 4.55a and Figure 4.55b for 700 ^{o}C and 850 ^{o}C samples, respectively. In inversion region, substantially lower leakage current than those of reference sample-1 and reference sample-2 were measured. However, in depletion region at gate voltage of V_{FB}, leakage currents are exceeding those measured in reference sample 1, but the sample obtained at 700 ^{o}C nitridation is still gives better leakage current at that region than the reference sample-2.

Theoretical C-V curves of W metal gate samples were also calculated using the experimental inputs of dielectric constant, oxide thickness, doping concentration of MOS capacitors. An example of ideal and experimental C-V curves normalized to oxide capacitance for both group of samples are presented in Figure 4.56a and Figure 4.56b for 700 ^{o}C and 850 ^{o}C nitrided samples, respectively. It is clearly seen from Figure 4.56 that there exist a significant flat band voltage shift for W metal gate samples as well. The values of V_{FB} for different dots are very close to 2.2±0.2 volt similar to those measured in reference sample-2 with Al metal gate and the same thermally grown Ta_2O_5 oxide layer. However, V_{FB} values showed large variations even on dots taken from the same substrate for MOS capacitor with RF sputtered Ta_2O_5 oxides and also with TiN metal gate with thermal Ta_2O_5 oxide layer. It is interesting that TiN metal gate has effect on both effective dielectric constant and calculated from oxide capacitance as well as the density of effective oxide charge. The N_{eff} values of W metal gate MOS capacitors are summarized in Table 4.10 and Table 4.11 for 700 ^{o}C and 850 ^{o}C nitrided samples, respectively. It is almost uniform around $60\pm12\times10^{11}$ cm^{-2} among different dots taken from the same substrate. It can be concluded that distribution of the effective oxide charge is more homogeneously distributed in W metal gate MOS capacitors.

The density of interface trap states of W metal gate samples were obtained from Terman's method in a similar way carried out for other groups of samples. D_{it} levels of MOS capacitors with prior nitridation process in N_2O at 700 ^{o}C and 800 ^{o}C are shown in Figure 4.7a and Figure 4.57b, respectively. D_{it} level for 700 ^{o}C nitrided sample is around $3\pm2\times10^{11}$ (eVcm^{2})$^{-1}$. These values are almost in the similar range of D_{it} levels measured for Al metal gates samples prepared with the same nitridation process in N_2O at 700 ^{o}C as presented in Figure 4.21. However, D_{it} levels for nitrided samples at 850 ^{o}C

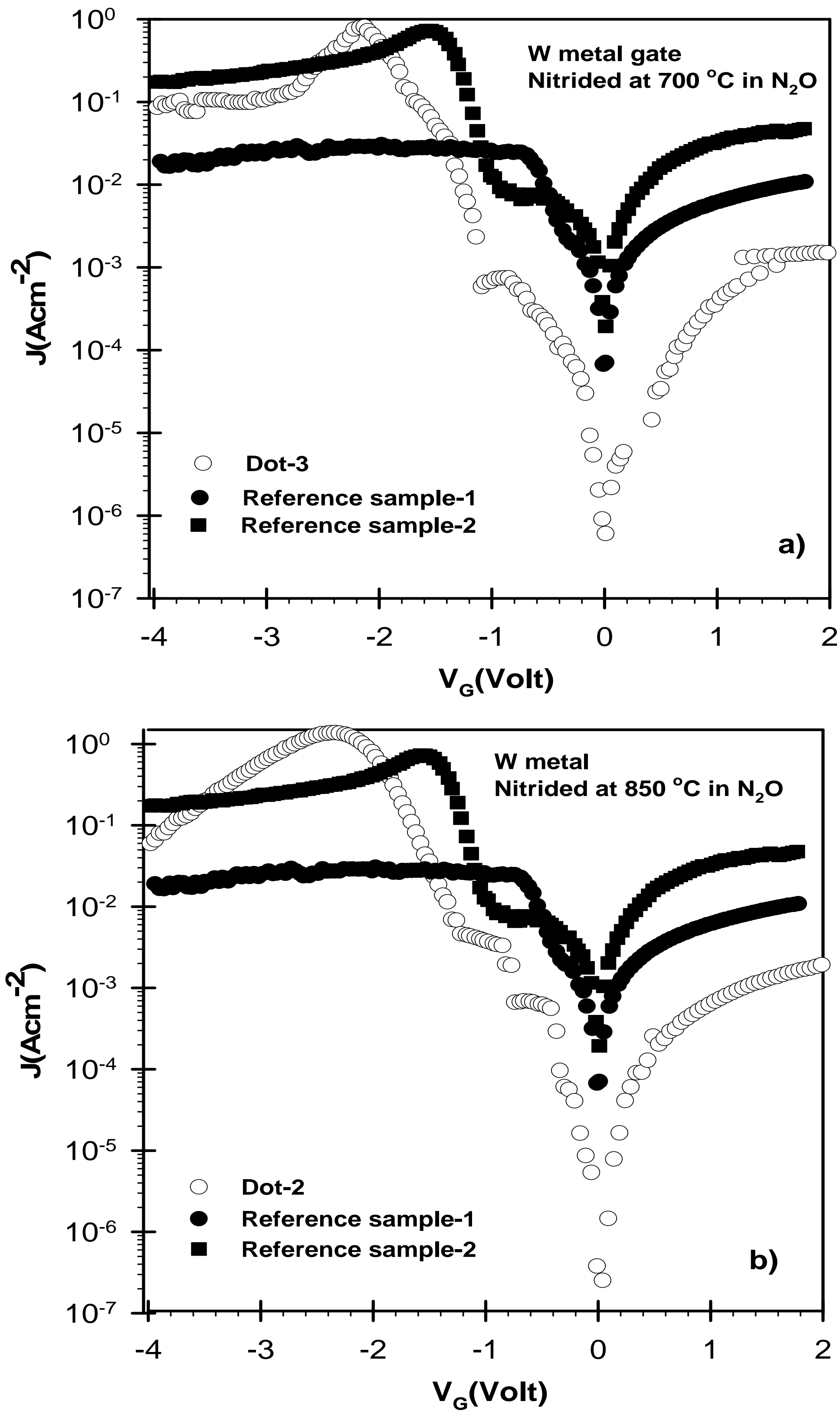


Figure 4.55. J-V characteristics of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O a) at 700ºC, b) at 850ºC

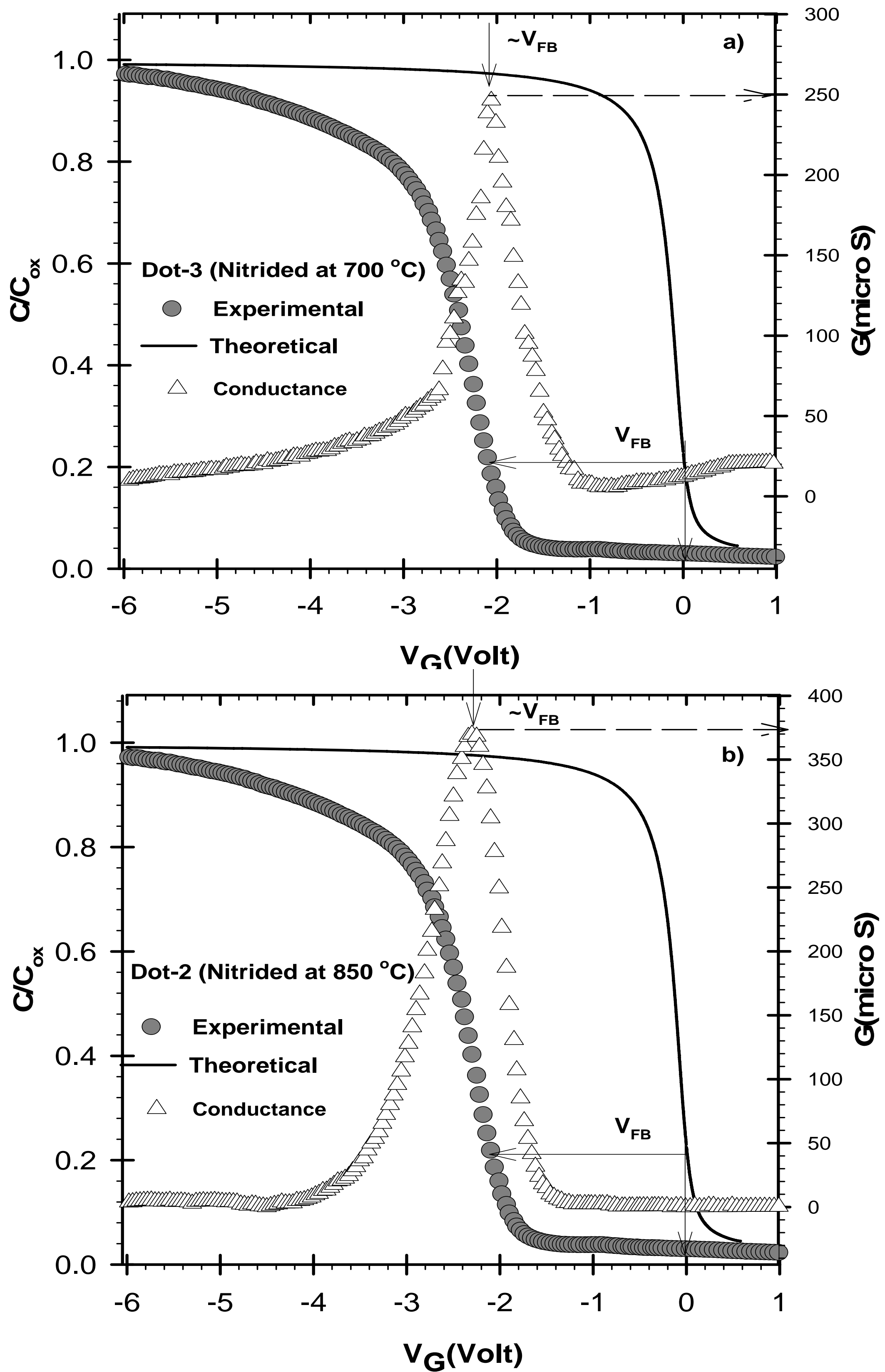
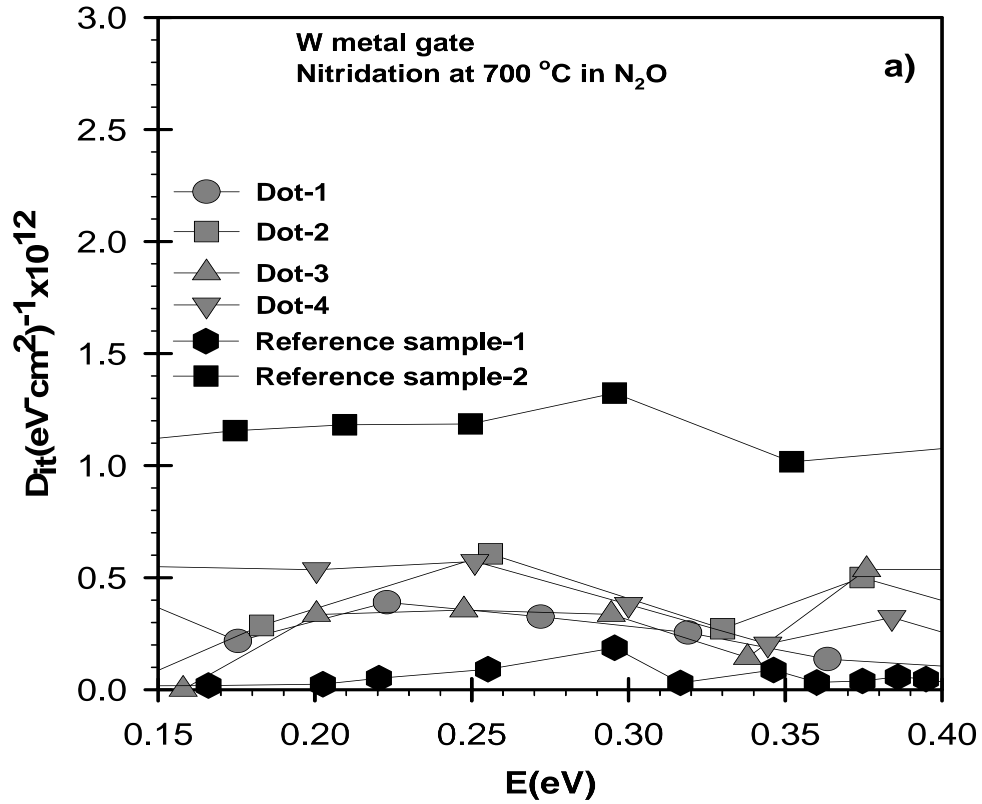


Figure 4.56. Normalized experimental and theoretical capacitance versus gate voltage and conductance versus gate voltage of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor prepared after nitridation process in N_2O at a) 700ºC, b) 850ºC



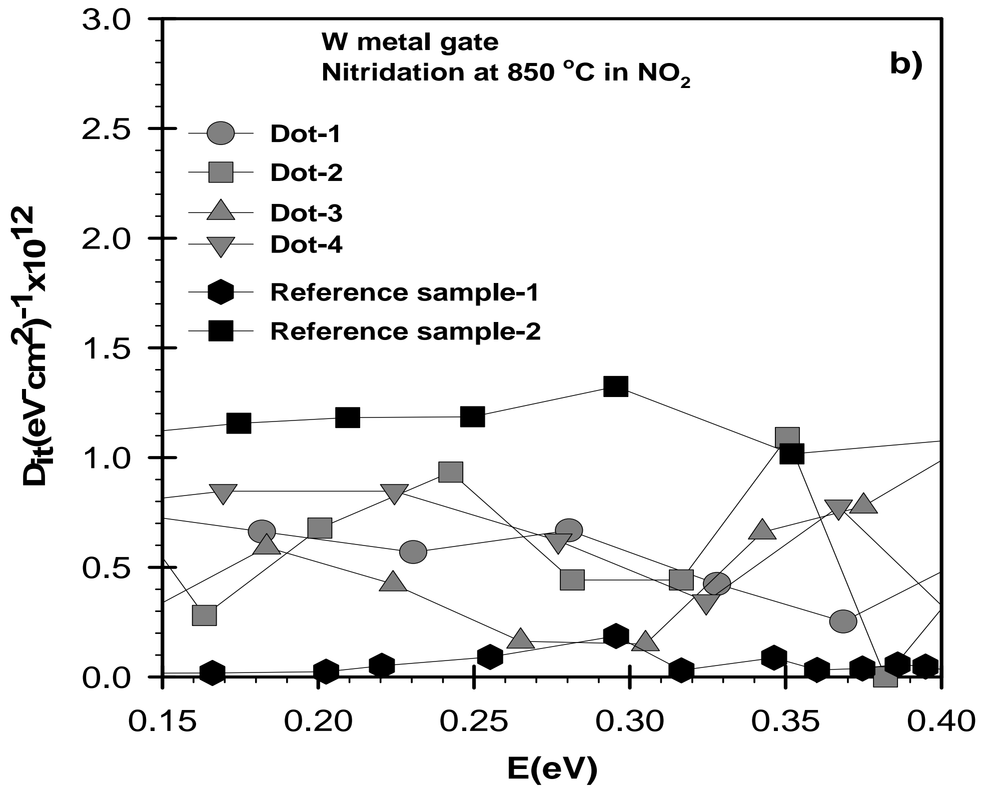


Figure 4.57. Density of interface states as a function of energy in the band gap of crystalline silicon for reference samples and four different dots of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor for nitridation in N_2O gas environment at a) 700°C, b) 850°C

show larger scattering and is around 5±4x10^{11} (eVcm^2)$^{-1}$. D_{it} levels for sample prepared with the same nitridation process at the same temperature with Al metal gate was measured to be 3±2x10^{11} (eVcm^2)$^{-1}$ as shown in Figure 4.28. D_{it} levels of W metal gate samples for different dots were also summarized in Table 4.10 and Table 4.11 for 700 ^{o}C and 850 ^{o}C nitrided samples, respectively.

Table 4.10. Summary of parameter extracted from experimental high frequency C-V measurements of W-Ta_2O_5-(SiO_xN_y)-Si-MOS capacitor prepared after nitridation process at 700ºC in N_2O gas ambient

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} (eVcm^2)$^{-1}$
Dot-1	22	6.25 x10^{-4}	11.8	298	-3	-2.33	-2.45	7.2	68	2±2
Dot-2			12.4	318	-2.4	-2.15	-2.2	6.9	70	4±2
Dot-3			12.09	302	-2.4	-2.3	-2.4	7.1	52	3±1
Dot-4			11.6	290	-3	-2.2	-2.3	7.4	66	4±2

Table 4.11. Summary of parameter extracted from experimental high frequency C-V measurements of W-Ta_2O_5-(SiO_xN_y)-Si-MOS capacitor prepared after nitridation process at 850ºC in N_2O gas ambient

Dot	t_{ox} (nm)	S (cm^2)	k	C_{ox} (pF)	Na (cm^{-3}) x10^{15}	V_{FB} (slope) (volt)	V_{FB} (shift) (volt)	t_{eq} (nm)	N_{eff} x10^{11} (cm^{-2})	D_{it} x10^{11} (eVcm^2)$^{-1}$
Dot-1	22	6.25 x10^{-4}	11.8	296	-5	-2	-2.1	7.2	47	5±1
Dot-2			12.3	308	-4.8	-2.3	-2.4	6.9	54	5±4
Dot-3			12.4	311	-5.5	-2.3	-2.4	6.9	75	4±3
Dot-4			12.5	315	-4.4	-2	-2.1	6.8	66	6±2

4.5.4 Conclusions

In the last part of thesis, the second objective, the effect of different metal gates on the characteristics of MOS capacitors, were investigated using three different gate metal, Al, TiN and W deposited on similar Ta_2O_5 oxide layers. Reference Sample 1 and Reference Sample 2 were also used for the comparison of the improvements in oxide and interface properties of MOS capacitors with different metal gates.

MOS capacitors in the form of Al- Ta_2O_5-(SiO_2)-Si and TiN-Ta_2O_5-(SiO_2)-Si have different metal gates but the same Ta_2O_5 formation process on silicon surface. There was no prior nitridation of silicon surface was carried out in these two group MOS capacitors. Only the effect of Al and TiN gate metals on the top interface of gate metal-gate oxide on the oxide and silicon-Ta_2O_5 interface quality were investigated from the high frequency C-V results. It was found that both group of samples showed very low level of moving trap charges as detected from the hysteresis C-V curves, with negligible ΔV_{FB} voltage shifts. It can be concluded that gate metal has no effect on the density of moving trap charges, which is mainly determined by the method of Ta_2O_5 oxide formation process. In both group thermal oxidation of Ta films in dry O_2 was used to form Ta_2O_5 oxide layers. However, there are major differences in dielectric constant, effective oxide charges and the density of interface traps between Al metal gate and TiN metal gates samples. Dielectric constant of 11.2 was observed for Al metal gate samples but it decreases to 6.2 for TiN MOS capacitors. The density of effective oxide charges is $3.0x10^{12}$ cm^{-2} for Al metal gate samples. It increases to 5.5 ± 1 x 10^{12} cm^{-2} for MOS capacitor with TiN gate metal. However, the density of interface traps improves significantly from 1.1 ± 1 $x10^{12}$ $(eVcm^2)^{-1}$ for Al metal gate to the level of $4\pm2x10^{11}$ $(eVcm^2)^{-1}$ for TiN metal gate MOS capacitors.

The effect of W gate metal on the characteristics of MOS capacitors were compared with the samples Al metal gate. Both group of samples had the same prior nitridation process of silicon surface in N_2O gas prior Ta_2O_5 oxide formation. In addition, deposition method of Ta_2O_5 was also identical. It was found that large hysteresis effect was observed in Al metal gate MOS capacitors. However, it is almost negligible for W metal gate samples. Dielectric constant for the same nitridation process is slightly lower for Al metal gate MOS capacitors indicating an interfacial layer formed at top interface by Al gate metal. For both nitridation temperatures, W metal gate

samples give almost identical dielectric constant with values around 12, which is significantly higher that those of Al metal gates. As the oxide and interface quality was compared, both Al and W MOS capacitors give similar values of high density of effective oxide charges and interface trap states.

CHAPTER 5

DISCUSSIONS AND CONCLUSIONS

High-k dielectric materials are important field of investigation for scaling down the electronic devices in today's microelectronic technology to replace native oxide SiO_2 used as gate oxide in DRAM applications. Using high-k dielectric layers for replacement of SiO_2 allow us to use physically thicker oxide layer to obtain the same oxide capacitance of conventional SiO_2 layer in devices with gate oxide below 50nm scale. This will provide low leakage currents through the gate oxide. In order to achieve such replacement of SiO_2, a new dielectric material must have higher dielectric constant than SiO_2, thermodynamically stable with silicon, low leakage currents and low level of effective oxide charges. Most of high-k dielectric materials have instability problem with silicon and resulting in rough interface between silicon and gate oxide and high level of interface trap density. In addition, high density of effective oxide charges and moving trap charges present in high-k oxide layers cause deterioration in device performance. Furthermore, the effective oxide thickness obtained with high-k oxide layer, EOT, is also determined from the top metal gate electrode used for the replacement of doped poly-silicon gate electrode. Since most of metal gate materials interact with underlying oxide layer and form very thin metal oxide at top interface in series with gate oxide with lower dielectric constant, which finally reduces the effective dielectric constant of high-k oxide layer. Therefore, it is imperative to investigate the effects of metal gates together with high-k oxide layers to replace native oxide SiO_2. In this thesis, tantalum pentoxide dielectric materials, Ta_2O_5, deposited on silicon substrate using different methods were investigated. In order to provide better interface with silicon substrate and a barrier between silicon and thermodynamically unstable high-k oxide layer, a prior nitridation of silicon surface in N_2O and NH_3 gas using rapid thermal nitridation process has been used before Ta_2O_5 oxide formation. The effects of prior nitridation process on interface quality of silicon- Ta_2O_5 structure were compared with unnitrided samples with the same Ta_2O_5 oxide layer and the same metal gate electrodes. In addition, three different metal gates, Al, TiN and W, were used with the same quality Ta_2O_5 oxide layers underneath. Their effects on oxide and interface properties of MOS capacitor with high-k oxide layers were investigated. In order to

compare the improvements in device characteristics by using different nitridation process and different metal gates, a reference sample, Reference Sample 1, with native oxide SiO_2 and a second reference sample, Reference Sample 2, with unnitrided silicon surface and Ta_2O_5 gate oxide were used. Both reference samples had Al metal gate electrodes. Characterization different MOS capacitors was performed using high frequency C-V method and effective dielectric constant, density of mobile trap charges, effective oxide charges and interface traps were obtained from the analysis of experimental and ideal C-V curves.

The characteristics of Reference Sample 1 were found that it had insignificant hysteresis shift in high frequency C-V curve with less than 30 mV ΔV_{FB} voltage shift, low density of effective oxide charges and very smooth Si-SiO_2 interface with D_{it} level of 1-2 x10^{11} cm^{-2} eV^{-1}. The same level of D_{it} were obtained from both Terman's method and the simultaneous C-V software. These values are very close to that reported for the best quality Si-SiO_2 interface (Manchanda et al. 1998). In Reference Sample 2, native oxide SiO_2 is replaced by thermally grown Ta_2O_5 high-k oxide layer with the same oxide thickness of 20nm. Effective dielectric constant increased to 12 as expected and hysteresis shift in high frequency C-V curve is still less than 30 mV ΔV_{FB}, required for good quality oxide layer. However, leakage currents are substantially higher, density of effective oxide charges and that of interface traps are one order of magnitude higher that that of reference Sample 1. This indicated that Ta_2O_5 creates very rough interface with silicon substrate and contains high density of oxide charges even though there is an improvement in effective dielectric constant. Such high value of oxide charges for Ta_2O_5 oxide layers are in good agreement with the reported results in the literature (Wilk, Wallace and Anthony 2001, Atanassova et al. 2002a).

In order to improve the stability of Ta_2O_5 oxide layer with silicon substrate, a novel approach called rapid thermal nitridation (RTN) process (Sun and Chen 1994) has been applied before high-k oxide formation. In this thesis, a prior nitridation process of p-type silicon surface in N_2O and NH_3 gasses at temperature between 700 ^oC and 850 ^oC was carried out before deposition of Ta_2O_5 oxide layers. All nitrided samples had the structure of Al-Ta_2O_5-(SiO_xN_y)-p-Si. Nitridation in N_2O were carried out at 700 ^oC, 800 ^oC, and 850 ^oC and nitridation in NH_3 was carried out at 700 ^oC and 800 ^oC. After that growth of Ta_2O_5 was carried out by using RF magnetron sputtering of Ta target in Ar and O_2 gas ambients. Finally, Al metal gates were evaporated using shadow mask with well defined gate areas.

The results of nitridation in N_2O for three different temperatures indicate that there is significant improvement in the interface quality between silicon and Ta_2O_5 interface from that of unnitrided Reference Sample 2. Here, nitridation process in N_2O creates very thin (1-2 nm) SiOxNy interfacial layer to protect silicon substrate from instable Ta_2O_5 oxide and thus low level of interface trap density. D_{it} levels obtained from several dots on the same substrate are very close to the value of (2-3) $\pm 1x10^{11}$ cm^{-2} eV^{-1} for three different nitridation temperatures. These values of D_{it} are very close to that measured for Reference Sample 1 with smooth gate oxide SiO_2. The obtained results for the D_{it} levels are in good agreement with the recent results given in the literature (Novkovski et al. 2005). Therefore, RTN is a promising process to integrate into silicon processing technology. However, there are major issues related to other non-ideal effects present in the gate oxide. First, effective dielectric constant k decreased to 6 for nitrided samples at 700 C and 800 C from the value of 12 of unnitrided Reference Sample 2. Then it increases to 10.3 for nitridation at 850 C. The increase in dielectric constant results in a decrease in EOT for samples at 850ºC. This can be attributed to highly stable SiO_xN_y formation on silicon surface, which prevents the interaction with Ta_2O_5 oxide layer. It was reported by Park et al. that formation of AlN_x as an interfacial layer between gate metal and gate oxide results in an increase in equivalent oxide thickness thus a decrease in oxide capacitance values (Park et al. 2003). On the other hand, according to Atanassova et al., Al react with Ta_2O_5 to form Al_2O_3 or Al suboxides. In our case, nitrogen might diffuse inside the oxide and to top interface of Al-Ta_2O_5 and there might results in a generation of AlN_x or Al_2O_3 interfacial layers for nitrided samples at 700 ^oC and 800 ^oC.

The second effect is that all nitrided samples in N_2O gas show large hysteresis C-V curves with ΔV_{FB} flat band voltage shifts between 30mV and 800 mV even on different dots taken from the same substrate. This indicates that there is a variation in the density of moving trap charges and most samples show large density of moving trap charges. The third effect is that leakage currents in depletion region around flat band voltage are much higher that that measured in reference Sample 1. The fourth effect is that flat-band voltage shift of experimental C-V curve from the ideal one is higher than Reference Sample 1 and it even shows variations among the dots taken from the same substrate. Consistent values of V_{FB} were obtained from both $1/C^2$ vs V_G and from the shift of ideal and experimental C-V curves as well as that obtained from the peak position of conductance versus gate voltage for each dot. The values of N_{eff} calculated

from the V_{FB} change between $2x10^{12}$ cm^{-2} and $5x10^{12}$ cm^{-2}, which are an order of magnitude higher than Reference Sample 1. The non-uniformity in the flat band voltage, thus in N_{eff}, can be attributed to non-uniform nitrogen penetration inside the oxide, since excessive nitrogen inside the oxide results in oxide charge defect, which in turn results in device instability as reported in the literature (Wristers et al. 1996). Moreover, another confirmation of non uniform nitrogen penetration towards the oxide layer is that the peak value of conductance, one of the most important parameter gate oxide, increased by several times above the level of Reference Sample 2 without any nitrided layer and reached to the values between 330 μS and 450μS. All nitrided samples in N_2O at three different temperatures exhibit the similar characteristics in terms of effective oxide charges and hysteresis effect. But preferred nitridation temperature could be 850 ^oC in N_2O since the highest effective dielectric constant of 10.3 and the lowest equivalent oxide thickness were obtained at this nitridation temperature.

In order to improve interface of silicon and Ta_2O_5, second nitridation process of silicon surface was performed using NH_3 gas at 700 ^oC and 800 ^oC. Nitrogen rich SixNy interfacial layer of 1-2nm has been formed on silicon. The samples were in the form of Al-Ta_2O_5-(SiO_xN_y)-Si. The highest dielectric constant of 12 was obtained for the samples nitrided at 700 ^oC and it decreases as nitridation temperature decreases. A main difference in C-V curve from those nitrided in N_2O is that C-V curve in accumulation region show two steps which is due to trapping on slow states as reported in literature (Novkovski et al. 2005). All samples nitrided at 700 ^oC and 800 ^oC show large hysteresis shift in C-V curves, the same as observed in those nitrided in N_2O gas. Therefore, it can be inferred that large hysteresis behavior could be due to the nitridation process or RF sputtering techniques of the oxide layer since both Reference Sample-1 and Reference Sample-2 were prepared with thermally grown Ta_2O_5 oxide layer and both exhibited insignificant hysteresis shifts.

Furthermore, high values of flat band voltage shifts V_{FB} and even large variation in V_{FB} were obtained among the dots taken from the same substrate, the same as observed in N_2O nitrided samples. Similar levels of effective oxide charges were also calculated in NH_3 nitrided samples as well. This could be due to both nitrogen and hydrogen diffusion towards oxide layer since this can cause high level of oxide charges and increases conductance through the gate oxide. In fact, the peak value of conductance curve for NH_3 samples are slightly higher than those measured in N_2O

nitrided samples as presented in conductance vs gate voltage figures. Finally, the density of interface traps for samples nitrided in NH_3 was lower than Reference sample 2. However, the D_{it} level for 700 ^oC nitrided sample shows a variation around $(4\pm3)x10^{11}$ $(eVcm^2)^{-1}$ and increases slightly to $(6\pm3)x10^{11}$ $(eVcm^2)^{-1}$ for 800 ^oC nitrided samples. These values are slightly higher than those of N_2O nitrided samples. The important note is that the interface between silicon and Ta_2O_5 oxide layer is not smoother than those obtained for N_2O nitrided samples. The interface is deteriorated in NH_3 nitridation. The reason for this could be due to the fact that N_2O nitridation provides oxygen rich SiO_xN_y which causes a decrease in the D_{it} levels at silicon-Ta_2O_5 interface. However, the presence of NH_3 gives raise to formation of nitrogen rich $SiO_xN_{y,}$ which increase the roughness of the interface.

In conclusion, these results of prior nitridation process indicate that nitridation process provide substantial improvement in interface properties of silicon-Ta_2O_5 high-k oxide. However, it does not improve the oxide charge properties such as moving trap charges and effective oxide charges and even the leakage current density. Moreover, with the uncontrolled nitridation process, the oxide charge properties can be worsened. Therefore, further investigation is needed to understand the nature of these oxide charges present in MOS devices with high dielectric constant materials.

The second objective of this thesis was to investigate the effects of different metal gates on overall performance of the MOS devices with high-k oxide layers. For this purpose, samples with three different metal gates were studied in detail. These are Al, TiN and W metal gates. The high-k Ta_2O_5 oxide layers underneath were maintained to be the same quality in order to see the effect of different metal gate on measured characteristics of MOS devices. The first group of samples has the form of Al-Ta_2O_5-(SiO_2)-Si (Reference Sample 2), the second group has the form of Al- Ta_2O_5-(SiO_xN_y)-Si, the third group of samples has the form of TiN-Ta_2O_5-(SiO_2)-Si and fourth group of samples has the form of W- Ta_2O_5-(SiO_xN_y)-Si structure. Here, the effects of Al and TiN metal gates were compared using MOS capacitors with the same thermally grown Ta_2O_5 oxide layer on silicon substrate. It was found that both group of samples have very low level of moving trap charges with insignificant ΔV_{FB} voltage shifts below 30mV in hysteresis C-V, high level of effective oxide charges and leakage currents. Major difference is that effective dielectric constant is 12 for Al metal gate sample and it is around 6 for TiN metal gate MOS capacitor. Both had the same gate area but Al metal gate sample has 20 nm and TiN sample had 15 nm oxide thickness. The result of

deterioration in effective dielectric constant for TiN samples could be due to strong interaction of Ti with underlying gate oxide, which then easily oxidizes the structure of TiN metal gate as reported in literature (Kwon et al. 1996). On the other hand, there is a significant improvement in the density of interface trap states at silicon- Ta_2O_5 interface for TiN metal gate samples. Both Al and TiN metal gate samples have the same thermally grown Ta_2O_5 oxide layer on silicon substrate. However, D_{it} levels are not in the same level. D_{it} level for TiN metal gate samples decreased to $(6\pm3)x10^{11}$ $(eVcm^2)^{-1}$ from 1.1 x 10^{12} $(eVcm^2)^{-1}$measured for Al metal gate sample. It was observed by Atanassova and Paskaleva that metal gate does not result in difference in D_{it} level. It was suggested that nitrogen break from Ti and penetrate inside the oxide and to the silicon- Ta_2O_5 interface. Finally, it might react with Si surface and results in a presence of an interfacial layer in the form of SiO_xN_y, which improves the D_{it} level. Similar type of observation was also partly supported by Green et al (Green et al. 2001).

The final gate metal used for the investigation was tungsten, W, due to its highest tensile strength and excellent corrosion resistance. It shows no inter diffusion with the surrounding materials and smooth interface with dielectrics. The fifth group of samples used in this thesis was prepared using W metal gate. In this group of samples, RTN process of silicon surface at 700 ^oC and 850 ^oC in N_2O was applied. Then, the Ta metal films were deposited by RF sputtering method. Dry oxidation of Ta film in O_2 at 873 ^oC was carried out to form high-k Ta_2O_5 oxide layer. Finally, W metal gate electrodes were deposited on the oxide using RF sputtering method. The effect of W metal gate was compared with samples having Al metal gate and the same prior nitridation process of silicon surface in N_2O gas at 700 ^oC and 850 ^oC. The results of these nitrided samples were already discussed above and will be summarized here for the comparison. The only differences is that the formation of Ta_2O_5 oxide layer in Al metal gate samples is made by RF sputtering of Ta target in Ar and O_2 gas. On the other hand, W metal gate sample has thermally grown Ta_2O_5 oxide layer from RF sputtered thin Ta film formed on silicon surface. Both group of samples had the same prior nitridation temperatures of 700 ^oC and 800 ^oC in N_2O gas.

Effective dielectric constants for Al metal gate samples are 6.9 anf 10.3 for 700 ^oC and 850 C nitrided samples, respectively. However, it is almost 12 for W metal gate samples for 700 C and 850 C nitrided samples. These lower values of dielectric constant could be due to interaction of Al metal gate with underlying Ta_2O_5 oxide layer and forming Al_xO_y suboxides layer in series with lower dielectric constant. This finally

reduces oxide capacitance and effective dielectric constant. However, W gate metal does not interact with gate oxide and almost identical dielectric constants were measured for both nitrided samples. Second major effect was measured in hysteresis effect of C-V curves. Almost insignificant ΔV_{FB} voltage shifts were measured for all dots of W metal gate samples. However, large ΔV_{FB} voltage shifts and variations among dots from the same substrate were measured for Al metal gate samples nitrided under the same conditions. This large ΔV_{FB} voltage shifts could not be due to metal gates but due to formation method of Ta_2O_5 oxide layer since W metal gate samples have thermally grown Ta_2O_5 oxide layer the same as Reference 2 and the samples with TiN metal gate. All has insignificant hysteresis shift in C-V curves.

Furthermore, the density of effective oxide charges calculated from the V_{FB} voltage shifts is still higher for both Al metal gate and W metal gate samples. This is the major effect of high-k Ta_2O_5 oxide layer independent of deposition method of oxide layer. These results are in good agreement with the reported results in the literature (Sjöblom, Westlinder, and Olsson, 2005, Green et al. 2001). However, the density of interface traps, D_{it}, is very close to the level of Reference Sample 1 with native oxide SiO_2. The density of interface traps changes between $3x10^{11}$ $(eVcm^2)^{-1}$ and $5x10^{11}$ $(eVcm^2)^{-1}$, which is mainly determined by the prior nitridation of silicon surface causing a smooth interface between silicon and Ta_2O_5 oxide layer. It can be inferred from the results of different metal gate samples that gate metal can interact with the underlying gate oxide and modify gate metal-gate oxide interface, which finally affects the general performance of MOS capacitor.

In order to understand the behavior of the metal gate on the oxide layer and to support our investigations about the reaction of the metals with the underlying oxide layer, Energy-Dispersive Analysis of X ray (EDX) was used to find quantitative information about the elements present at a determined point away from the metal gate area. The point was selected as a point where there is no formation of MOS capacitor and contains only Ta_2O_5 oxide on Si surface as shown in Figure 5.1. At that specified point, EDX results should not contain any metal concentration. However, according to the EDX results, the quantitative measurement of Al, Ti, N and W elements for that point is not zero. It indicates a lateral diffusion of those elements through the oxide layer as shown in Figure 5.2, 5.3 and 5.4 respectively. The diffusion of Al and Ti and the breaking of nitrogen from TiN which were observed in EDX results is a further confirmation to our investigations. However, the diffusion of W was surprising and

implies that if more controlled formation method of W is succeeded, even better electrical characteristics can be obtained for the sample with W metal gates.

Based on these results, it can be concluded that, the use of metal gate on high-k dielectric material used in DRAMs introduces its own capacitor quality challenges. As the electrical characteristics of Ta_2O_5 film with different metal gate analyzed, it was obtained that, EOT, current density, flat band voltage and dielectric constant were all highly depended on the gate metal while hysteresis and interface characteristics are depend on the high-k dielectric materials deposition technique. Therefore, the more general conclusion is that, the choice of the gate material and deposition technique of the high-k for DRAMs application is a critical concern for high-k dielectric materials. More investigations are required to resolve such critical issues present in high-k oxide layers.

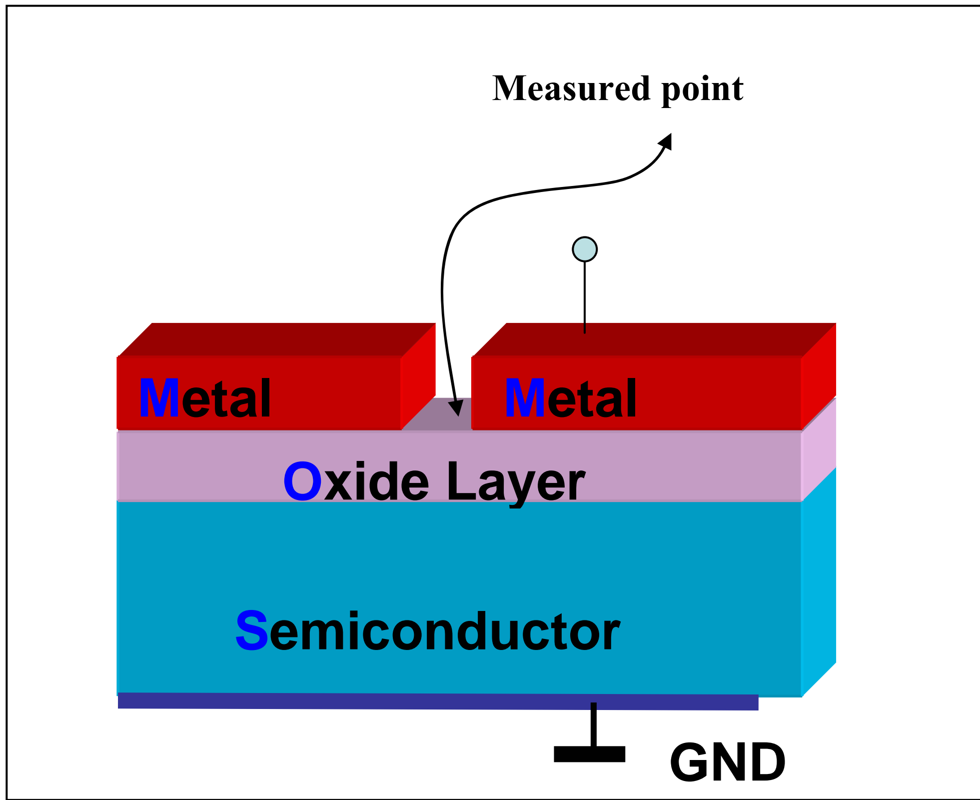


Figure 5.1. Schematic representation of the point where the EDX measurement was carried out

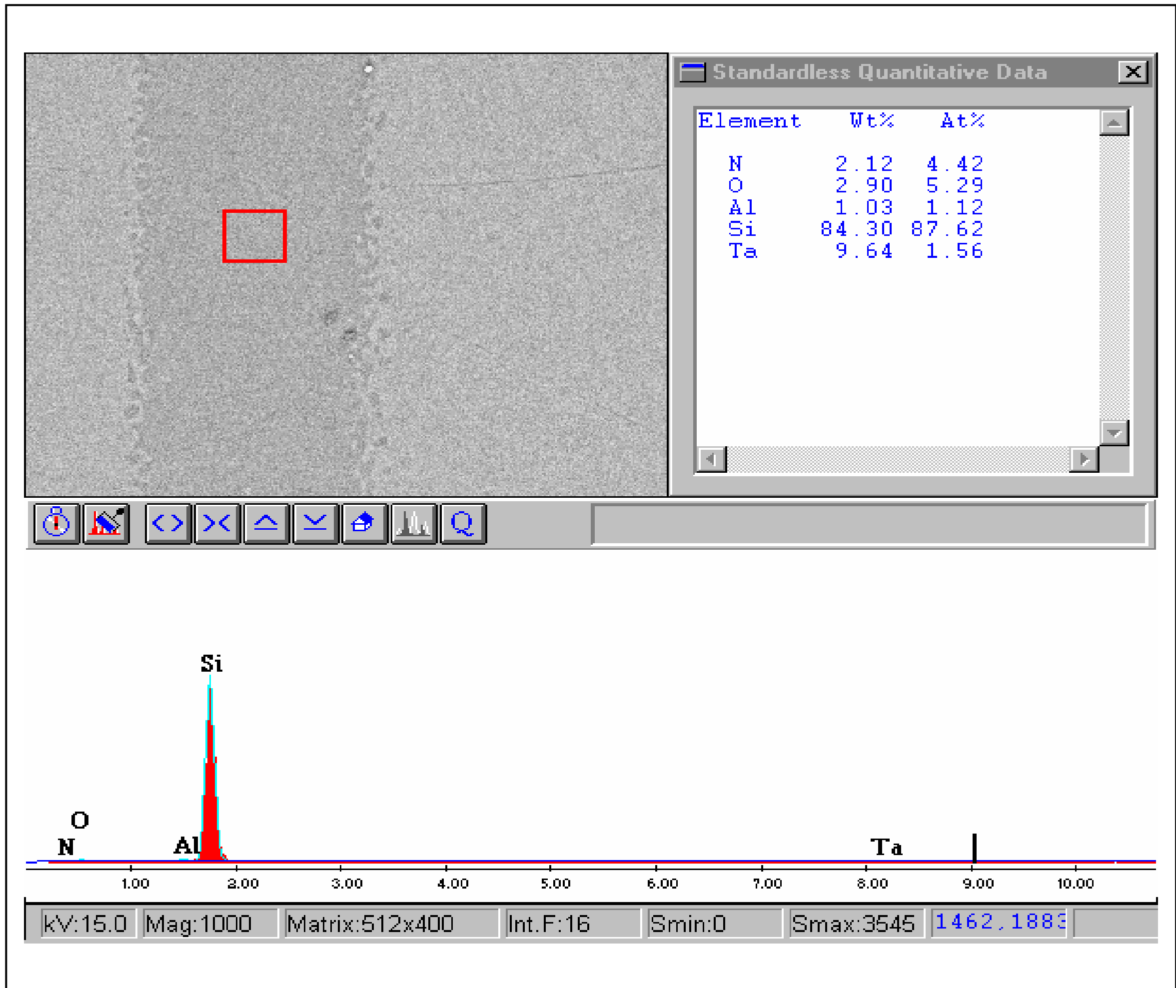


Figure 5.2. EDX result of sample prepared at 700 ^{o}C in N_2O in the form of Al-Ta_2O_5-(SiO_xN_y)-Si MOS,

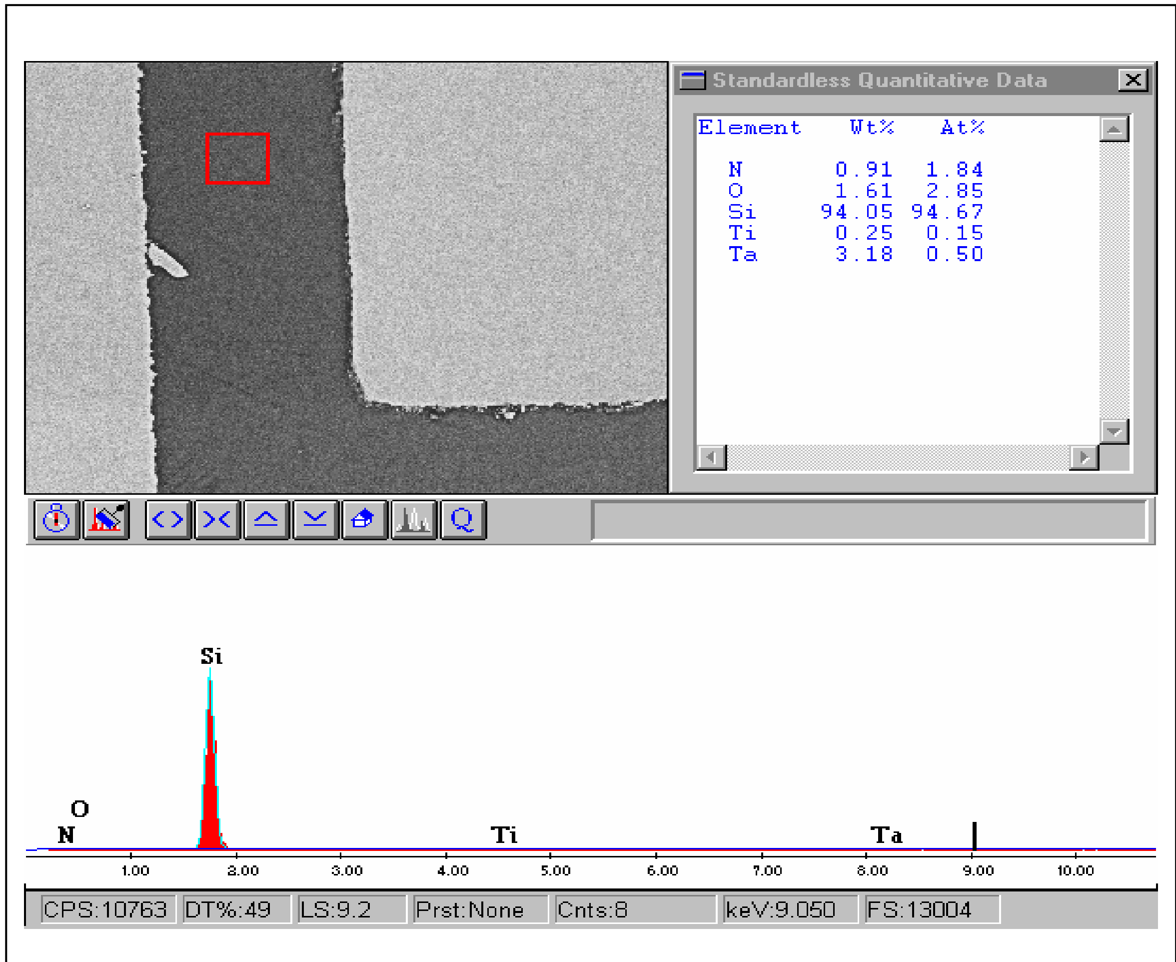


Figure 5.3. EDX result of sample prepared in the form of TiN-Ta_2O_5-(SiO_2)-Si,

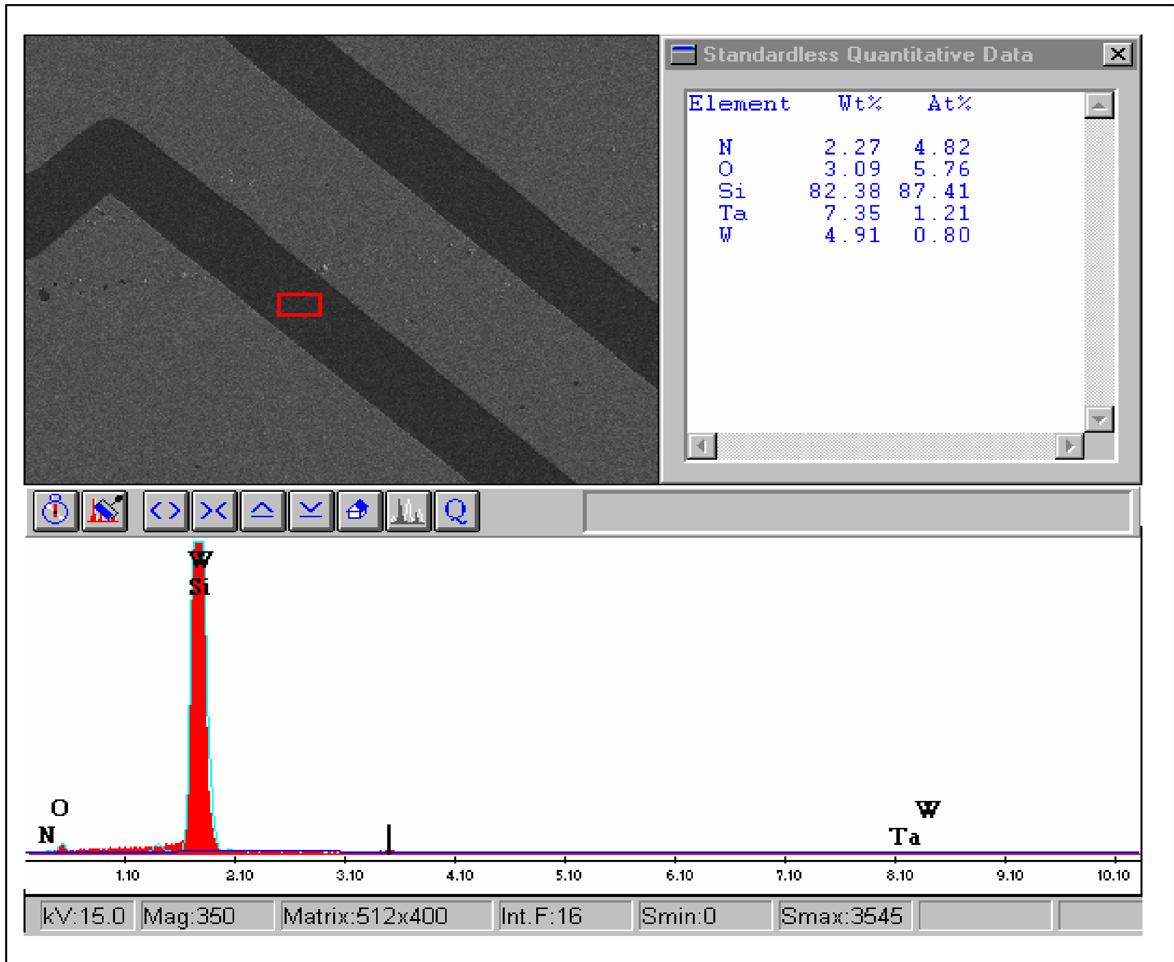


Figure 5.4. EDX result of sample prepared at 700 °C in N_2O in the form of W-Ta_2O_5-(SiO_xN_y)-Si MOS capacitor

5.1 Future work

In this thesis, it was found that a prior nitridation process in N_2O and NH_3 gas is a promising method for improving silicon- Ta_2O_5 interface, especially nitridation at 850 ^oC in N_2O and nitridation in NH_3 at 700 ^oC gives better interface and higher dielectric constants. However, formation of Ta_2O_5 using RF magnetron sputtering from Ta target in Ar and O_2 gas causes large hysteresis effect. Instead thermal oxidation of Ta films in dry oxygen could be oxide formation method since no moving trap charges exists in those oxide layer It is soft growth process in contrast to the magnetron sputtering of Ta target. Investigations should focus on improving device processing conditions to decrease the levels of effective oxide charges and leakage currents to the level of native oxide SiO_2 by keeping the high dielectric constant and better interface properties. In addition, non-interacting gate metal candidate could be tungsten. The research for the gate metal and high-k dielectric should be carried out together in order to solve complex problems together.

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