Analysis of interface states of the pentacene organic thin-film phototransistor by conductance technique

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ABSTRACT

A pentacene thin-film transistor with a channel width of 300 μm and a channel length of 30 μm has been successfully fabricated on n-Si substrate with thermally oxidized SiO_2 as a gate insulator. The photovoltaic and interface state density properties of the transistor have been investigated. A pentacene film of 200 nm thickness was deposited on the SiO_2 layer with a vacuum thermal evaporator. Atomic force microscopy images of the pentacene film on SiO_2 insulating layer show a homogeneous film surface with the rms roughness of 11 nm. The transistor shows p-channel characteristics, as a result of positive carriers generated in the pentacene film for the negative bias voltages applied to the gate.

The photosensitivity (I_{ph}/I_{dark}) is measured as 1.45 at an illumination intensity of 3500 lux at the off state. This suggests that the pentacene thin-film transistor shows a phototransistor characteristic. The field-effect mobility of the pentacene OTFT was found to be 0.021 $cm^2/(V s)$. The interface state density of the transistor was determined using conductance technique and was found to be about 1.191×10^{10} eV^{-1} cm^{-2}.

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1. Introduction

Organic thin-film transistors (OTFTs) have been extensively investigated in recent years and steady progress in performance of these devices has been realized [1–7]. OTFT devices have been used in low-cost, large-area, flexible electronic applications such as all-polymer integrated circuits [8,9], polymer-dispersed active-matrix displays [10–12], large-area sensor arrays [13,14], biochemical sensors [15] and radio frequency identification tags [16]. The active layer of an OTFT is usually made of a thin film of highly conjugated n-channel [17,18] or p-channel [19–21] small molecules, such as perfluorinated copper-phthalocyanine (F16-CuPc) [22] or pentacene [23,24]. Among these organic molecules, pentacene ($C_{22}H_{14}$) has the highest carrier mobility (more than 5 $cm^2/(V s)$) and on/off ratio [25,26] when used a semiconducting transport layer for OTFTs [27–29] and optoelectronic devices [30–32], making it one of the most promising organic semiconductors. Pentacene consists of stacked molecular layers arranged in a herringbone structure with interplanar spacing $d_{001} = 14.1$ Å [33]. Van der Waals forces are effective between its molecular layers [34,35]. Several techniques, such as photoelectron emission microscopy (PES) [36], potential imaging mapping [37], and scanning Kelvin probe microscopy (SKPM) [38,39] have been used to probe local defects originating from structural disorders, crystalline domain size, shape, and height of the pentacene layer itself. Metastable defects under bias voltage using space-charge limited current spectroscopy [40], deep charge traps using electric force microscopy [41] and shallow traps by using scanning tunneling microscopy (STM) [33] have been observed to clarify the charge transport mechanism at the interface between pentacene and insulating dielectric layers on various substrates [42]. The field-effect mobility and performance of an OTFT device depend also on deposition rate and substrate temperature that affect the morphology and molecular ordering of semi-crystalline organic semiconductors like pentacene [43,44].

Optical response of pentacene in the UV and visible regions is promising for use in phototransistor applications [45,46]. Combination of light detection and signal amplification in a single device without noise problems [47–49] gives superior performance to pentacene-based OTFTs for photo-sensor applications [50,51].

In this work, we have prepared a pentacene thin-film transistor with top contact geometry as an optical sensor to investigate the photo-sensing characteristics of the device under the illumination of visible light. Furthermore, our aim is to show whether the interface states that are formed during the fabrication of the pentacene thin-film transistor are effective on the device characteristics. To this end, we have characterized the interface states using the conductance-frequency method.

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2. Experimental

A top contact thin-film transistor (OTFT) has been fabricated with a p-channel organic semiconductor pentacene with 98% purity, purchased from Sigma–Aldrich. An n-type (N/Phos) single crystal silicon wafer pre-polished on one side and having a ⟨1 0 0⟩ surface orientation, thickness of 530 mm, diameter of 100 mm and 2.00 Ω-cm resistivity was purchased from Si-Mat Silicon Wafers Company, and used as a substrate. A 250 nm thick SiO_2 layer was thermally grown by annealing of an n-type Si wafer substrate for 1 h at 1250 °C in a pure oxygen atmosphere and used as a gate dielectric layer of the OTFT device. A 200 nm thick pentacene film was deposited on the SiO_2 layer with a vacuum evaporator and was used as the active layer of the organic thin-film transistor. A gold metal thin film (purity 99.95%) with a thickness of 200 nm was thermally evaporated from a tungsten filament under 6×10^{-6} Torr vacuum. Gold top contacts on the n-Si/SiO_2/pentacene structure were formed having a channel length of 30 μm and channel width of 300 μm using a shadow mask. Fig. 1 shows the schematic diagram and optical microscopy images of the OTFT structure used in this work. The current–voltage characteristics ($I_{ds} - V_{ds}$ and $I_{ds} - V_{gs}$) of the OTFT were measured with a KEITHLEY 2400 Sourcemeter and a KEITHLEY 6517 Electrometer. The capacitance–frequency, capacitance–voltage and conductance–frequency characteristics of the pentacene OTFT transistor were measured at the gold contacts (area of 0.14625 cm^2) using a HIOKI 3532 LCR meter (Bohemia, USA). Photovoltaic measurements were employed using a 200 W halogen lamp. The morphology of the pentacene thin film as deposited on the SiO_2 dielectric surface was examined with a Solver P47H
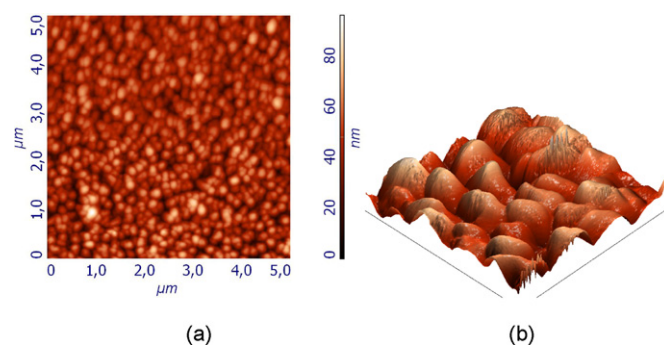

Fig. 2. Atomic force microscopy (AFM) images of pentacene film on SiO_2: (a) 2D image with 5 μm × 5 μm scan size; (b) 3D image with 1 μm × 1 μm scan size.

atomic force microscope (NT-MTD) (Moscow, Russia) operating in tapping mode in air at room temperature. Diamond-like carbon (DLC) coated NSG01_DLC silicon cantilevers (from NT-MTD) with a 2 nm tip apex curvature were used at its resonance frequency of 150 kHz. The Nova 914 software package was used to control the SPM system and for the analysis of the AFM images.

3. Results and discussion

3.1. Output characteristics of the pentacene thin-film transistor

The two-dimensional and three-dimensional atomic force microscopy (AFM) images of a pentacene film deposited on a SiO_2 dielectric surface are shown in Fig. 2a and b, respectively. The AFM image shows a homogeneous pentacene film surface with the root-mean-square (rms) roughness of 11 nm. As seen from Fig. 2(a), the pentacene grains on SiO_2 form ellipsoidal particle shapes with aspect ratio of 150 nm/200 nm. The grain size may be attributed to the wetting properties of the dielectric layer. Pentacene films with larger grain sizes yield higher carrier mobilities [52,53].

Fig. 3 shows the drain current–voltage curves of the transistor under different gate voltages. As seen in Fig. 3, the OTFT device indicates a clear p-channel transistor behavior, since positive carriers are generated in the pentacene organic semiconductor layer upon application of negative gate voltages. The drain current I_d increases with V_{ds} and saturates at higher voltages when the gate voltage is varied between −15 and 15 V. The drain current usually tends to saturate due to the pinch-off of the accumulation layer if the drain voltage V_{ds} is more negative than the applied gate voltage V_{gs}. At
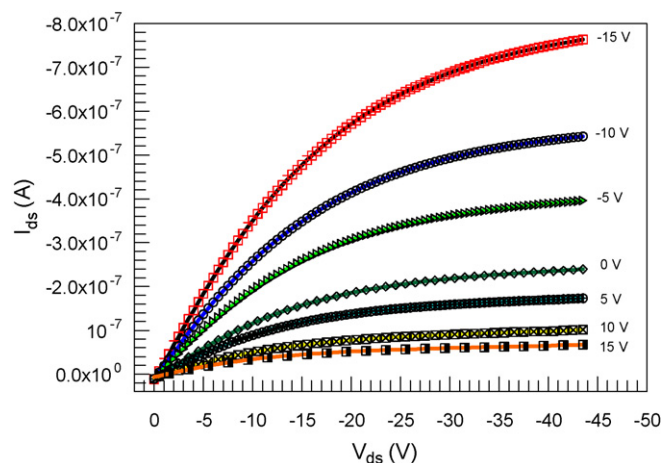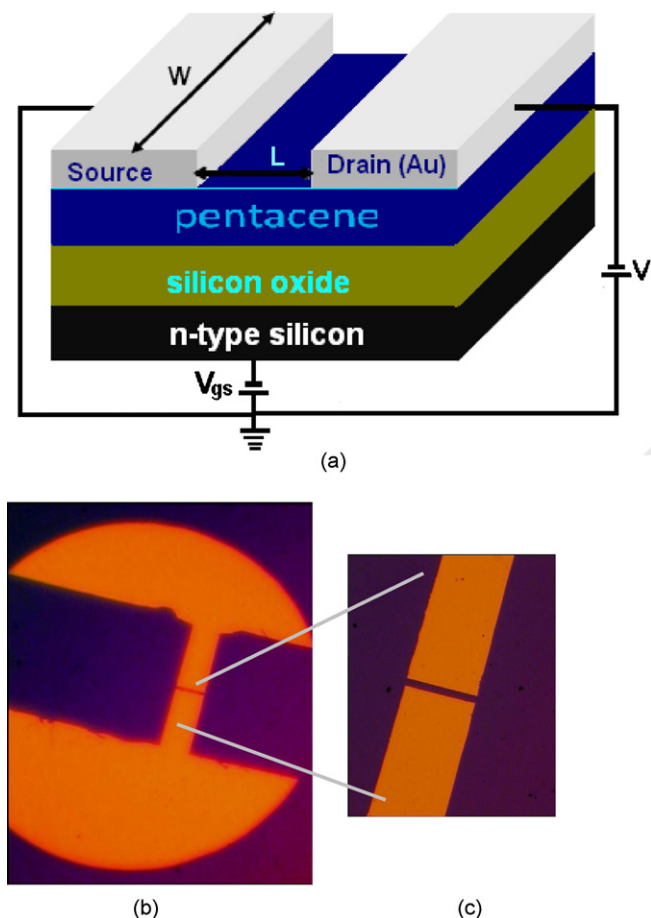

Fig. 1. (a) Schematic structure of OTFT; (b and c) optical microscopy images of n-Si/SiO_2/pentacene/Au OTFT device.
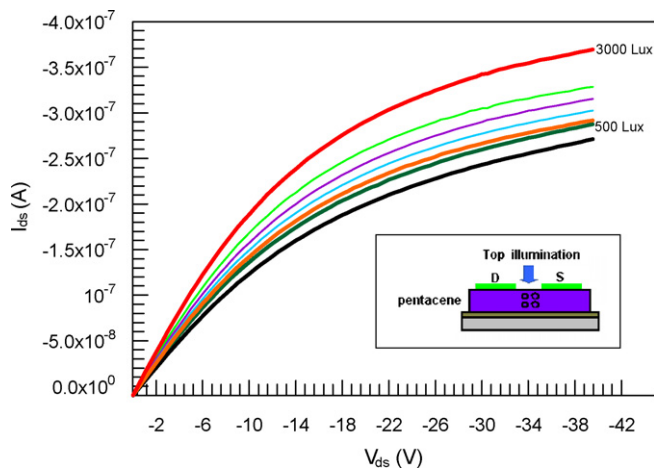

Fig. 3. Output characteristics of the pentacene thin-film transistor at different gate voltages.

Fig. 4. Output characteristics of the pentacene thin-film transistor at various illumination intensities for $V_g = 0$ V.

Fig. 5. Plot of $I_{ds}^{1/2} - V_g$ of the pentacene thin-film transistor.

lower voltages, the drain current–voltage curves exhibit good linearity of response. This confirms that a good ohmic contact has been established between the pentacene and gold contacts.

Fig. 4 shows the drain–current curves of the pentacene thin-film transistor under various illumination intensities from 500 to 3000 lux, using a tungsten filament white light source. Accordingly as seen in Fig. 4, the transistor is thus sensitive to illumination intensity in the visible white light range. This suggests that the pentacene thin-film transistor shows phototransistor characteristics. The drain current of the transistor increases with increasing illumination intensity. The photosensitivity (I_{ph}/I_{dark}) was measured as 1.45 at an illumination intensity of 3500 lux under $V_g = 0$. This value is low. Liu et al. [54] have found that the photosensitivity of polymer thin-film transistors based on poly(2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylene vinylene) depends on the gate voltage. In the study made by Liu et al., when using the above-threshold mode, the on-state current increased slightly under illumination and the photosensitivity (I_{ph}/I_{dark}) is 1.93 at an illumination intensity of 1200 lux and a gate voltage of −25 V. However, for the sub-threshold mode, the off-state current significantly increases with illumination intensity and the maximum photosensitivity (I_{ph}/I_{dark}) is 198 ± 17 at the same illumination intensity and a gate voltage of −5 V [54]. These results indicate that the photocurrent of an OTFT is modulated by the gate voltage.

The drain current in the linear region can be expressed by [55]

$$I_{ds} = \frac{W}{L} \mu C_i \left[(V_g - V_{th})V_d - \frac{V_d^2}{2} \right] \tag{1}$$

where I_{ds} is the drain-source current, W is the width of channel, L is the channel length, C_i is the capacitance of the oxide layer, V_g is the gate voltage, μ is the mobility and V_{th} is the threshold voltage. On the other hand, the drain current in the saturation region can be expressed by [56]

$$I_{ds} = \frac{W}{2L} \mu C_i (V_G - V_{th})^2 \tag{2}$$

Fig. 5 shows the curve of $I_{ds}^{1/2} - V_g$ for the pentacene OTFT transistor. The field-effect mobility and threshold voltage of OTFT from $I_{ds}^{1/2} - V_g$ plot were found to be 0.021 cm²/(V s) and 28.88 V, respectively. The results of the measured mobilities of the pentacene OTFT transistors studied in this work and in Refs. [57,58] suggest that the preparation process of the pentacene layer is very sensitive. Especially, the deposition rate has critical effects on the charge transport and the interface properties of the pentacene transistor.
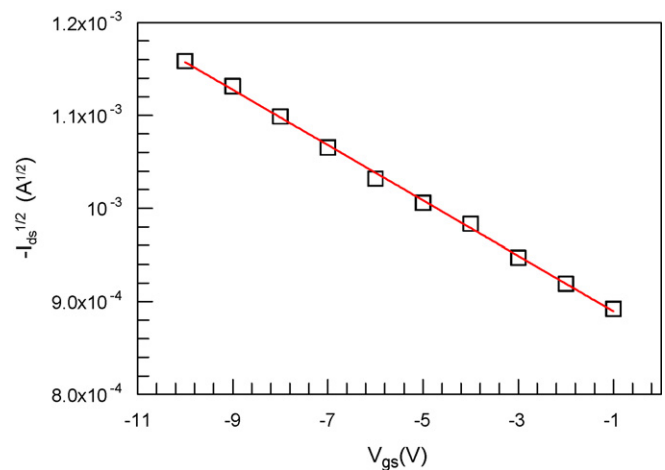
3.2. Interface state density properties of the pentacene thin-film transistor

Since pentacene-OTFTs exhibit higher drain-source currents (I_{ds}) at negative applied gate voltages, our attention focused on the capacitance–voltage (C–V) response at these voltages (Fig. 6). As the applied negative gate voltage is increased, the capacitance increases slightly and reaches a constant value. The oxide layer capacitance for the transistor was determined from the C–V curve and was found to be 8.20 nF/cm². This capacitance value obtained for a 250 nm thick SiO₂ layer is in agreement with oxide layer capacitance values obtained by others for SiO₂ layers (6.91 nF/cm² for 500 nm SiO₂ layer and 11.5 nF/cm² for 300 nm SiO₂ layer) [59,60].

The capacitance–frequency (C–f) characteristics of the pentacene OTFT transistor have been measured in order to evaluate the presence of a continuous distribution of the interface states in the pentacene layer. Fig. 7 shows the measured capacitance as a function of the frequency of the transistor at 0.0 and 2 V bias voltages. The capacitance of the transistor increases with decreasing frequency and tends to be constant. At lower frequencies, the capacitance is resulting from interface states following the alternating current signal (AC). Whereas, at higher frequencies, the interface states in equilibrium with the semiconductor do not contribute to the capacitance, since the charge at the interface states cannot follow the applied AC signal.
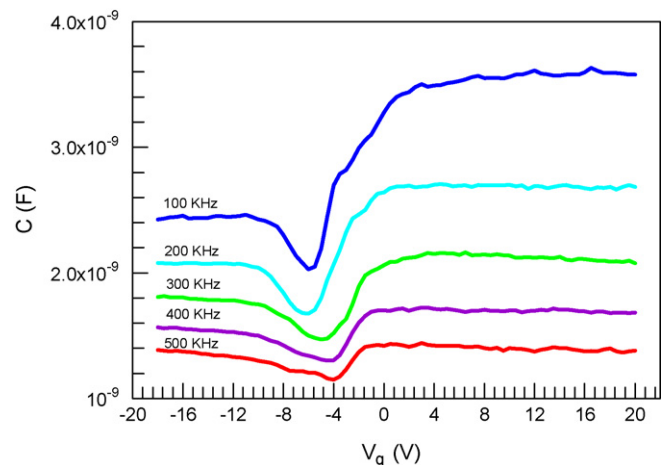

Fig. 6. The capacitance–voltage curves of the pentacene thin-film transistor at different frequencies.
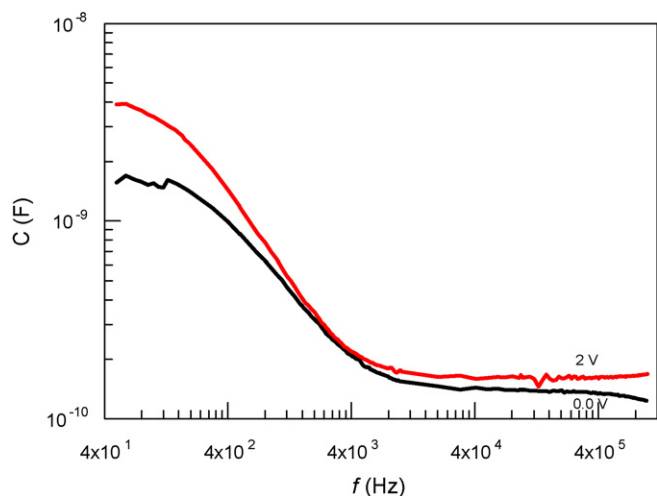
Fig. 7. The capacitance–frequency (C–f) characteristics of the pentacene thin-film transistor at different voltages.

Fig. 8. Plots of (G/ω) versus f of the pentacene thin-film transistor at different voltages.

Admittance spectroscopy has been used for the interface trap analysis obtained from electrical properties of the metal–insulator–semiconductor devices. The complex admittance expression for the interface trap states can be defined as follows:

$$Y = G_p + i\omega C_p \tag{3}$$

where G_p and C_p are the real and imaginary parts of the admittance, respectively. The G_p and C_p relations is expressed by the following relation [61]:

$$G_p = \frac{C_{it}}{2\tau} \ln(1 + \omega^2 \tau^2) \tag{4}$$

$$C_p = C_d + \frac{C_{it}}{\omega\tau} \arctan(\omega\tau) \tag{5}$$

where $C_{it} = qAD_{it}$, C_{it} and D_{it} are the interface state capacitance and density, respectively, and A is the diode contact area, ω is the angular frequency and τ is the time constant of the interface states. The parallel capacitance and conductance expressions in terms of the measured capacitance C_m and conductance G_m are defined as follows:

$$C_p = \frac{-(G_m/\omega)^2(1/C_{ox}) + C_m(1 - (C_m/C_{ox}))}{(G_m/\omega C_{ox})^2 + (1 - (C_m/C_{ox}))^2} \tag{6}$$

and

$$G_p = \frac{G_m}{(G_m/\omega C_{ox})^2 + (1 - (C_m/C_{ox}))^2}, \quad \text{respectively.} \tag{7}$$

If Eq. (4) is rearranged, the interface state conductance can be written as

$$\frac{G_p}{\omega} = \frac{qAD_{it}\tau}{2\omega\tau} \ln(1 + \omega^2\tau^2). \tag{8}$$

The maximum value of Eq. (4) is obtained by taking $\left| d(G_p/\omega)/d(\ln w) \right| = 0$ where the maximum condition is found to be $\omega\tau = 1.98$. This value is substituted into Eq. (4) and the interface state density is calculated by the following relation:

$$D_{it} = \frac{(G_p/\omega)_{\max}}{0.402qA}. \tag{9}$$

The plots of (G/ω) versus $\log f$ for the transistor are shown in Fig. 8. The peaks present in the plot can be explained as the existence of a continuous distribution of the interface states. As seen in Fig. 8, the peak position shifts to higher frequencies with 2 V bias voltage. This indicates a variation of the interface state density with an applied voltage. The interface state density for the
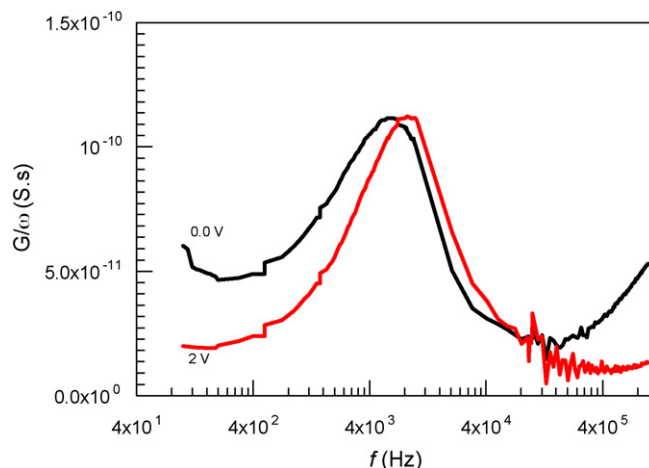
transistor was determined from Fig. 8 and was found to be about 1.191×10^{10} eV^{-1} cm^{-2}. The obtained D_{it} value for the transistor studied is lower than that of organic field-effect transistors fabricated with pentacene as the active material and different polymeric dielectrics such as cyanoethylpullulan, poly(4-vinyl phenol), polymethylmethacrylate, parylene-C and polyimide as the gate material [62]. The obtained D_{it} value is a low value. This suggests that the interface states at this density are not effective on the device characteristics. Therefore, it is suggested that the interface states of organic thin-film transistors are effectively influenced by gate material.

4. Conclusions

The photovoltaic and interface state density properties of the pentacene thin-film transistor fabricated on an n-Si substrate with thermally oxidized SiO$_2$ as a gate insulator have been investigated. The OTFT transistor showed p-channel characteristics and a photosensitivity (I_{ph}/I_{dark}) of 1.45 at an illumination intensity of 3500 lux during the off state. The field-effect mobility and the interface state density of the pentacene OTFT were found to be 0.021 cm^2/(V s) and 1.191×10^{10} eV^{-1} cm^{-2}, respectively.

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