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THE EFFECTS OF OXIDE THICKNESS ON THE INTERFACE AND OXIDE PROPERTIES OF METAL-TANTALUM PENTOXIDE-SI (MOS) CAPACITORS

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High dielectric constant tantalum-pentoxide insulating layers were prepared on p-type (100) crystalline silicon wafers using an RF magnetron sputtering technique. Then, metal-oxide-semiconductor (Al-Ta_2O_5-Si) structures were formed with various oxide thickness from 15 to 25 nm. Devices were characterized using the high frequency capacitance-voltage (C-V) spectroscopy method. From the analysis of the high frequency C-V curves, non-ideal effects such as oxide charges and interface trap densities have been evaluated. The results for Ta_2O_5 layers have been compared with those for conventional SiO_2 layers. Interface trap densities were found to be $1.6 \pm 0.4 \times 10^{12}$ eV^{-1} cm^{-2} for Ta_2O_5 and about 2×10^{11} eV^{-1} cm^{-2} for SiO_2 insulating layers. There was no clear thickness dependence of the interface trap densities for the Ta_2O_5 insulating layers.

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Keywords: Metal-oxide-semiconductor (MOS) capacitors, Tantalum pentoxide, Capacitance-voltage spectroscopy

1. Introduction

High dielectric constant insulating layers have become important to replace the native silicon dioxide used for the gate dielectric of DRAMS [1, 2 and references therein]. The search for a replacement for SiO_2 not only requires a high dielectric constant but also chemical stability with Si, a low leakage current and wide band gap properties. Among all the candidates, Ta_2O_5 layers have received considerable attention because of their potential application as dielectric films for storage capacitors in high density DRAMs [3-6] due to the relatively high dielectric constant (20-40), high refractive index and adequate dielectric breakdown strength [7 and references therein, 8]. It has also been demonstrated that the dielectric constant of Ta_2O_5 layers shows a thickness dependence [7-10]. Nevertheless, there are a number of problems that have to be overcome before sufficient reliability can be provided in modern integrated circuit fabrication. One of them is the defect density in the structure of the Si-Ta_2O_5 interface and that in the oxide. In general, these defect states in the SiO_2 system are characterized qualitatively, using high frequency capacitance-voltage measurements and quantitatively by using the conductance spectroscopies [11]. However, in high dielectric constant insulators, the investigation of these defect states is rather difficult, due to high leakage currents through the oxide. In the present paper, the effects of the oxide thickness on the interface properties of Si-Ta_2O_5 structure are investigated using the high frequency C-V characteristics of Al-Ta_2O_5-Si(p) (MOS) structures and the effective oxide charges and interface trap densities are obtained using Terman's method [12].

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2. Experimental procedure

Tantalum pentoxide films with thicknesses of 15 – 25 nm were deposited on p-type (100), 15 Ω cm Si, by RF magnetron sputtering from a tantalum target in an Ar atmosphere. The system base pressure was 6×10^{-4} Pa, the working gas pressure 3 Pa, the RF power density 2.2 W/cm^2, the deposition rate, ν = 9.3 nm/min, and the substrate temperature T_s = 300K. After the deposition, the Ta films were oxidized in dry oxygen at atmospheric pressure at 873 K with an O_2 flow rate of 5.1 min^{-1}. It is proposed that the oxidation temperature, Tox, is low enough for oxidation of the silicon substrate to be negligible, and the formation of tantalum silicide is prevented. The thickness t_{ox} of the Ta_2O_5 layers was measured by ellipsometry (λ = 632.8 nm) and layers with t_{ox} = 15, 20 and 25 nm were investigated. For the electrical characterization, MOS capacitors were fabricated by evaporation of Al dots with a thickness of 500 nm, through a shadow mask with a gate electrode area of 1.96×10^{-3} cm^2. Post metallization annealing was carried out in H_2 at 723 K for 1h. High frequency C-V measurements were carried out using a Keithley Model 82 system, and the data were acquired by a computer through an IEEE-488 interface bus. The dielectric constant, doping concentration and flat band voltage values were determined from the experimental high frequency C-V curves. Theoretical ideal C-V characteristics were calculated using a computer program and equations defined for MOS devices [13,14]. The effective oxide charge density ,$N_{eff,}$ and the density of interface defect states, Dit, were calculated from the high frequency C-V curves using Terman's method [12,14].

3. Results and discussion

The experimental high frequency C-V characteristics of Al-Ta_2O_5-Si(p) (MOS) capacitors with different oxide thicknesses are shown in Fig. 1. These curves represent the typical high frequency C-V dependence of a MOS capacitor. The doping concentrations of the devices are almost identical (2×10^{15} cm^{-3}), as obtained from the $1/C^2$ vs. V_G curves. The flat-band voltages, V_{FB}, due to non-ideal effects present in MOS capacitors, were found to be -1.74, -1.77 and -1.63 V for oxide thicknesses of 15, 20 and 25 nm, respectively. The effect of the oxide thickness is clearly reflected in the magnitude of the oxide capacitance dominating in the accumulation region, since the areas of the devices are equal and the dielectric constant did not change significantly at these oxide thicknesses. The parameters derived from the high frequency C-V measurements are also summarized in Table 1, where the dielectric constant, ε_{ox}, of Ta_2O_5 is 11.7 ± 0.9, in agreement with recent reports [7-10]. In addition, the experimental high frequency C-V curves of an Al-SiO_2-Si MOS capacitor prepared on a p-type Si wafer with a 1.17×10^{15} cm^{-3} doping concentration is shown in Fig. 1, to compare the effect of the dielectric constant of Ta_2O_5 layers on the oxide capacitance. For the same 20 nm oxide thickness and gate area, the oxide capacitance of the Al-SiO_2-Si(p) MOS capacitor shifts to lower values due to the different dielectric constant.

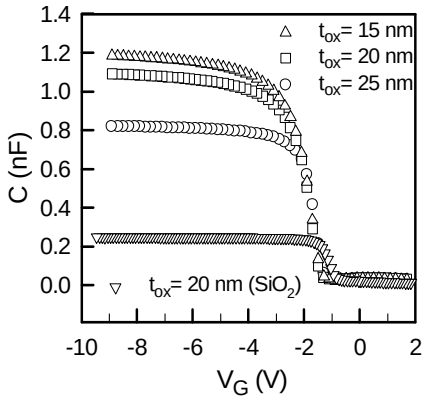

Fig. 1. High frequency (1MHz) capacitance-voltage characteristics of Al-Ta_2O_5-Si (MOS) capacitors with different oxide thicknesses, and that of conventional Al-SiO_2-Si capacitor with an oxide thickness of 20 nm.

Table 1. Summary of the parameters extracted from the high frequency C-V measurements. Data presented here are the average of several device characteristics measured from different parts of the substrate wafer

Sample	tox (nm)	ε_{ox}	C_{ox} (pF)	Na (cm^{-3}) $\times 10^{15}$	V_{FB} (volt)	N_{eff} (cm^{-2}) $\times 10^{12}$
Ta_2O_5	15	10.1	1165	2.04	-1.74	3.11
	20	12.6	1093	1.95	-1.77	3.02
	25	11.8	818	2.15	-1.63	1.90
SiO_2	20	3.9	250	1.17	-1.31	0.34

The theoretical capacitance versus surface potential, ψ_s, was calculated using the corresponding theoretical equations defined for MOS capacitors [13,14] and the extracted experimental values of the doping concentration, N_A, oxide thickness, dielectric constant and gate area. Both the experimental and theoretical (ideal) normalized capacitance (C/C_{ox}) versus gate voltage data are plotted together in Fig. 2, for insulating layers of Ta_2O_5 and SiO_2. It is clearly seen that the experimental normalized C-V curve shifts from the ideal one, due to non-ideal effects present in the MOS devices. The flat-band voltage, V_{FB}, values obtained for each sample are also indicated on the normalized capacitance curves. Using these voltage shifts, the effective oxide charge density, Q_{eff}, and effective number of charges per unit area, N_{eff}, are calculated using equation (10.10) of reference [14]. These are also summarized in Table 1. For oxide layers of thickness 15 and 20 nm, N_{eff} is about 3.1×10^{12} cm^{-2} and decreases to 1.90×10^{12} cm^{-2} for a 25 nm thick Ta_2O_5 layer. The level of N_{eff} found here is in the same order as reported for the other metal oxide layers proposed for the replacement of SiO_2 [1]. However, N_{eff} is 3.4×10^{11} cm^{-2}, approximately ten times lower than for native oxide SiO_2, in agreement with reported results [1].

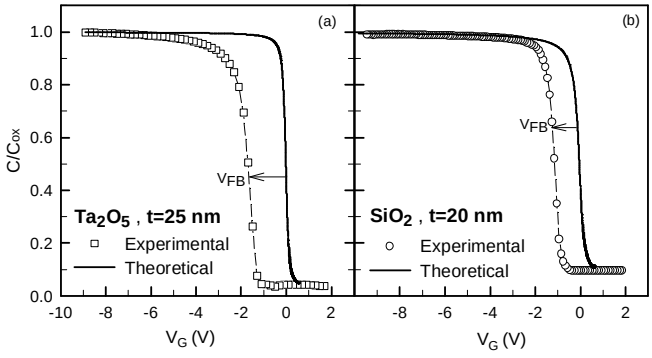

Fig. 2. Normalized experimental and theoretical capacitance-voltage curves of MOS capacitors with an insulating layer of (a) Ta_2O_5 and (b) SiO_2.

In addition, the shifts between the theoretical and experimental curves are not only due to oxide charges but also to states at the oxide-Si interface. Using the theoretical and experimental normalized capacitance curves, the surface potential ψ_s versus gate voltage V_G curve was obtained for each sample, and the density of interface trap states, D_{it}, was calculated using Terman's method [12]. The distribution of D_{it} values obtained for the Ta_2O_5 and SiO_2 insulating layers is shown in Fig. 3, as a function of the energy in the bandgap of the silicon. The value of D_{it} for Ta_2O_5 is $1.6\pm0.4\times10^{12}$ cm^{-2} eV^{-1}, and does not show a clear dependence on the oxide thickness.

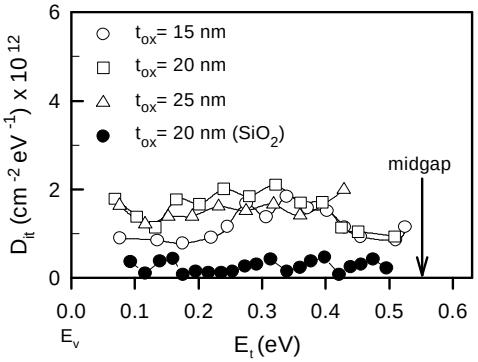

Fig. 3. Density of interface trap states as a function of energy in the bandgap of c-silicon for Ta_2O_5 and SiO_2 insulating layers.

However, these values are much higher than that of native oxide SiO_2, and are above the limit for the requirement of D_{it} ($< 2\times10^{11}$ cm^{-3} eV^{-1}), as specified by a detailed investigation [1] of the possibilities for the replacement of the gate dielectric in technological applications, for device dimensions of less than 50 nm.

4. Conclusions

The use of of Ta_2O_5 insulating layers, less than 30 nm thick, in MOS capacitors was examined in terms of the oxide and Si-oxide interface properties, which were investigated using high frequency C-V spectroscopy. They were compared with those of native SiO_2 insulating layers. It was found that Ta_2O_5 layers contain almost ten times higher concentrations of effective oxide charges than native oxide SiO_2. The density of traps at the Si-Ta_2O_5 interface is about $1.6 \pm 0.4\times10^{12}$ cm^{-2} eV^{-1}, and does not show a systematic dependence on the oxide thickness. The values of D_{it} are still much higher than that of the SiO_2-Si interface and above the limit for the requirement of D_{it} ($< 2\times10^{11}$ cm^{-3} eV^{-1}) as specified by a detailed investigation [1] of the possibilities for the replacement of the gate dielectric in technological applications, for device dimensions of less than 50 nm.

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