High-mobility pentacene phototransistor with nanostructured SiO$_2$ gate dielectric synthesized by sol–gel method

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Abstract

We have fabricated a pentacene based phototransistor by employing a modified nanostructured SiO$_2$ gate dielectric. The photosensing properties of the pentacene thin film transistor fabricated on n-Si substrate with nanostructured SiO$_2$ as gate dielectric have been investigated. The photocurrent of the transistor increases with an increase in illumination intensity. This suggests that the pentacene thin film transistor behaves as a phototransistor with p-channel characteristics. The photosensitivity and responsivity values of the transistor are 630.4 and 0.10 A/W, respectively at the off state under AM 1.5 light illumination. The field effect mobility of the pentacene phototransistor was also found to be 2.96 cm$^2$/Vs. The nanostructured surface of the gate possibly is the cause of the high-mobility value of the phototransistor due to light scattering from the increased surface area.

1. Introduction

Sputtering and thermal chemical vapor deposition (CVD), are common techniques to create a smooth insulating gate films for normal organic and inorganic field-effect transistors. Light-trapping plays a key role for crystalline Si thin film solar cells and phototransistors. The application of textured glass substrates instead of planar glass substrates is an attractive way to implement light trapping [1,2]. Several techniques are used to fabricate textured rough surface on transparent conductive oxide (TCO) glasses for solar cell applications. A simple chemical etching step in diluted acid, yields a textured surface which can be adjusted to give optimal light scattering over a wide wavelength range. Rech et al. showed that ZnO:Al films prepared by magnetron sputtering and post deposition wet chemical etching demonstrate an effective light trapping and the textured surface reduces reflection losses at the ZnO:Al/Si-interface with excellent light scattering properties for silicon thin film solar cells and modules [3,4]. Grained polycrystalline silicon (poly-Si) films were prepared on nano-textured glass substrates by epilaxial thickening of seed layers formed by the aluminum-induced layer exchange (ALILE) process [5,6] for poly-Si thin film solar cell application with 8% efficiencies with improved material quality [7–10].

The insulating film which plays the role of the gate in a phototransistor needs to combine high capacitance for low level leakage and an adequate surface texture to introduce light scattering and subsequent light trapping to increase photo sensitivity by increasing the number of excited photo carriers. For efficient light trapping, the substrate textures should be in the order of the incoming light wavelength.

The sol–gel method for the synthesis of inorganic nanoparticles such as ZnO, TiO$_2$ and SiO$_2$ [11–15] has become one of the most popular chemical procedures. The reason of this popularity stems from the fact that sol–gel synthesis is easy and it is carried out at ambient or slightly elevated temperature. Indeed, the sol–gel method has led to the synthesis of a great variety of materials, the range of which is continuously expanding. A typical sol–gel route for making silicon oxide matrices and thin films is followed by hydrolysis of alkoxides, for example, alkoxysilanes. However, a review of the recent literature reveals an increasing interest in another sol–gel route based on organic acid solvolysis of alkoxides [16–18]. As it has been earlier found by Pope and Mackenzie [19] and later verified by others [20], organic (for example, acetic) acid solvolysis proceeds by a two step mechanism which involves intermediate ester formation. Simplified reaction schemes showing gel formation either by hydrolysis or organic acid solvolysis are...
presented by the following reactions. (in the following reactions only one of the four alkoxy groups is taken into account for reasons of simplicity, while acetic acid (AcOH) is chosen to represent organic acids in organic acid solvolysis):

Hydrolysis  \( \text{Si} - \text{OR} + \text{H}_2\text{O} \rightarrow \text{Si}-\text{OH} + \text{ROH} \)  
(1)

Acetic acid solvolysis  \( \text{Si} - \text{OR} + \text{AcOH} \rightarrow \text{Si}-\text{OAc} + \text{ROH} \)  
(2a)

\( \text{ROH} + \text{AcOH} \rightarrow \text{ROAc} + \text{H}_2\text{O} \)  
(2b)

\( \text{Si}-\text{OAc} + \text{ROH} \rightarrow \text{ROAc} + \text{SiOH} \)  
(2c)

\( \text{Si}-\text{OR} + \text{Si}-\text{OAc} \rightarrow \text{ROAc} + \text{Si}-\text{O} - \text{Si} \)  
(2d)

R is a short alkyl chain (for example, methyl, ethyl or isopropyl). Hydrolysis (1) produces highly reactive hydroxide species Si–OH, which, by inorganic polymerization, produce oxide, i.e. Si–O–Si that is the end product of the sol–gel process. More complicated is acetic acid solvolysis (2) where several different possibilities may define different intermediate routes to obtain oxide. Occurrence of reaction (2b) would mean that gel formation would proceed by an intermediate hydrolysis caused by water created through (2b). Reaction (2c) would create highly reactive Si–OH which would form oxide, while reaction (2d) directly leads to oxide formation. The sol–gel precursor used in the present work is not a simple alkoxide but a hybrid precursor that consists of a polyether chain with two triethoxysilane end groups covalently bound by urea bridges (ureasil), as can be seen in Scheme 1. This material was used because it helps to make very uniform nanocrystalline films on silicon wafers even after calcinations at high temperature to remove any of the organic material producing pure SiO2 which was finally the insulating material for the gate of the phototransistor.

Besides, optical response of pentacene in the UV and visible region is promising for use in phototransistor applications [21,22]. Combination of light detection and signal amplification in a single device without any noise problems [23–25] gives superior performance to pentacene based organic thin film transistors (OTFTs) for photo sensor applications [26]. As a consequence, organic field-effect phototransistors play an interesting role in the electronic devices technology, since they can be used for light induced switches, light triggered amplification, detection circuits and, in photOFET arrays for highly sensitive image sensors [27].

In this work, we present the fabrication of a high-mobility pentacene phototransistor (2.96 cm²/Vs), employing nanostructured SiO2 gate dielectric which was synthesized by sol–gel method, to investigate the photosensing characteristics of the device under visible light illumination.

2. Experimental

A top contact thin film transistor (OTFT) has been fabricated with a p-channel organic semiconductor pentacene with 98% purity, purchased from Sigma–Aldrich. An n-type (N/Phos) single crystal silicon wafer pre-polished on one side with <1 0 0> surface orientation, thickness of 530 μm, diameter of 100 mm and 2.00 Ω cm resistivity was purchased from Si-Mat Silicon Wafers Company, and used as a substrate. The Si-wafer was covered with a thin SiO2 layer with thickness 200 nm which was prepared by the sol–gel technique. All chemicals used in the sol–gel method have been purchased from Aldrich.

The hybrid organic/inorganic precursor used in the preparation of SiO2 thin films is presented in Scheme 1 and it was synthesized as following: Two different unhydrized alkoxysilane-polyether precursors were prepared as in previous publications [18,27].

Poly(propylene glycol)bis(2-aminopropanol) of molecular weight 230 and 3-isocyanatopropyltrimethoxysilane (ICS) (molar ratio [ICS]/[diamine]=2) were mixed in tetrahydrofuran (THF) under reflux (64 °C) for 6 h. The isocyanate group of ICS reacts with the amino groups of poly(propylene glycol)bis(2-aminopropanol) (acylation reaction) producing urea connecting groups between the polymer units and the inorganic part. After evaporation of THF under vacuum, a viscous precursor was obtained, which is stable at room temperature for several months. The abbreviated name of the thus prepared precursor used in the present work is ICS-PPG230.

2.1. Sol–gel synthesis and film deposition

Two grams of the ICS-PPG230 precursor was mixed with 2 g of ethanol. After stirring for 5 min, acetic acid (AcOH) was added and the mixture was stirred for about 5 h. Finally, thin films of composite organic–inorganic materials were formed on silicon wafers of desired size with spin-coating technique at a speed of 3000 rpm. The Si substrates were previously cleaned with sonication consecutively in a bath of ethanol and acetone. A thin and optically uniform film of SiO2 was obtained after calcination at 500 °C in a furnace, suggested that all organic content was eliminated. The furnace temperature was incremented at a ramp rate of 15 °C min⁻¹; this temperature was held for 15 min and then silicon wafers were cooled to room temperature. The film thickness of SiO2 film was approximately 200 nm according to SEM cross-sectional images.

A 200 nm thick pentacene film was deposited on the SiO2 layer under vacuum after thermal evaporation and it was used as the active layer in the organic thin film transistor. A gold thin film (purity, 99.95%) with a thickness of 200 nm was thermally evaporated from a tungsten filament under 6 × 10⁻⁶ Torr vacuum. Gold top contacts on the n-Si/SiO2/pentacene/Au OTFT device were formed having a channel length of 30 μm and channel width of 300 μm using a shadow mask. The schematic structure of n-Si/nano-SiO2/pentacene/Au OTFT device is shown in Fig. 1. The current–voltage characteristics \( (I_{ds}–V_{ds}) \) and \( I_{ds}–V_{gs} \) of the OTFT were measured with a KEITHLEY 2400 Source meter and a KEITHLEY 6517 Electrometer. Photovoltaic measurements were employed using a 200 W halogen lamp.

The morphology of the pentacene thin film as deposited on the nano-SiO2 dielectric surface was examined with a Solver P47H Atomic Force Microscope (NT-MTD) operating in tapping mode in air at room temperature. Diamond-like carbon (DLC) coated NSG01-DLC silicon cantilevers (from NT-MTD) with a 2 nm tip apex curvature were used at its resonance frequency of 150 kHz.

![Scheme 1. Chemical structure of ureasil precursor (ICS-PPG230 and n ~ 3).](image-url)
The Nova 914 software package was used to control the SPM system and for the analysis of the AFM images.

3. Results and discussion

In order to improve the working properties of pentacene thin film transistor, we modified the surface properties of the SiO2 dielectric layer using SiO2 nanoparticles formed by sol–gel fabrication technique. For the surface morphology of the dielectric layer, the two-dimensional and three-dimensional atomic force microscopy (AFM) images of SiO2 dielectric surface formed with sol–gel method and pentacene film deposited on the SiO2 were obtained by AFM as they are shown in Fig. 2a and b. The AFM image shows a homogeneous pentacene film surface with the root-mean-square (rms) roughness of 7.5 nm. As seen from Fig. 2a, the pentacene grains on SiO2 form ellipsoidal particle shapes with aspect ratio of 70 nm/90 nm. The grain size may be attributed to the wetting properties of the dielectric layer. The surface roughness of the SiO2 gate dielectric have an important effect on the performance properties of the dielectric layer. The surface roughness of nanostructured SiO2 layer may be attributed to the wetting mechanism. Table 1 shows the AFM data obtained from the surface analysis of n-Si covered with/without the nanostructured SiO2 surface roughness elimination. The effective mobility in polycrystalline materials depends on phonon scattering, impurity scattering, interface roughness scattering, defect scattering, and grain boundary scattering mechanisms [30,31]. The roughness of the studied transistor is in agreement with that obtained for another transistor structured also with pentacene [29]. We evaluated that the nanostructure of SiO2 gate dielectric contributes to the high performance of pentacene field-effect transistor. The higher mobility of the transistor can be attributed to the morphology of pentacene film on the nanostructured gate material and the dielectric/surface properties of transistor. As seen in AFM images, the transistor in our studies appears a relatively smooth surface with small roughness. This suggests that the mobility is improved by surface roughness elimination. The effective mobility in polycrystalline materials depends on phonon scattering, impurity scattering, interface roughness scattering, defect scattering, and grain boundary scattering mechanisms [30,31]. The roughness of the studied transistor is lower than that of pentacene phototransistors referred in literature [29,32] and thus, the higher mobility of the transistor depends on the surface roughness of the SiO2, as the mobility is improved by reduction in surface scattering mechanisms taken place in the presence of a smoother interface.

The threshold voltage for the transistor can be defined as follows [33–35],

\[ V_{th} = \frac{q}{C_i} \left( \frac{n}{d} \right) \]

where \( q \) is the electronic charge, \( n \) is the density of majority carriers and \( d \) is the thickness of the organic semiconductor. The density of majority carriers for the transistor was determined using Eq. (3) and was found to be \( 1.64 \times 10^{16} \text{ cm}^{-3} \).

The inverse sub-threshold slope for the transistor is expressed as follows: [35],

\[ S = \left[ \frac{d \log(i_d)}{d V_g} \right]^{-1} \]

The value for the transistor was determined from Fig. 4 and was found to be 3.98 V/dec. This value is a measure of the turn-on speed of the transistor and it indicates the presence of trap behavior and interface quality between the dielectric and active layer [35]. The value of the present transistor is higher than that pentacene transistor proposed in literature [29]. We finally evaluate that the studied transistor give a higher mobility with a smaller S value, which exhibits better performance.

The interface trap density for the transistor can be calculated by the following relation [36,37]:

\[ D_{it} = \frac{[\log(e)]}{kT/q} \frac{C_i}{q} \]

where \( k \) is the Boltzmann constant, \( T \) is the temperature, \( q \) is the electronic charge and \( C_i \) is 7.45 nF/cm\(^2\). With \( C_i \) and \( S \) values, the \( D_{it} \) was calculated to be \( 3.02 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1} \). The \( D_{it} \) value of the studied transistor is in agreement with that obtained for another pentacene transistor [29]. Fig. 5 shows the drain current curves of the pentacene thin film transistor under various illumination conditions. As seen in Fig. 5, the drain–source current of

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the transistor increases with illumination due to the flow of mobile carriers in the channel layer of the transistor via source–drain voltage. This confirms that the pentacene thin film transistor is a phototransistor. The photosensitivity \( \frac{I_{\text{ph}}}{I_{\text{dark}}} \) at 29 V was measured as 630.4 at an illumination intensity of 100 mW/cm² under

**Fig. 2.** Atomic force microscopy (AFM) images of SiO₂ dielectric surface formed with the sol–gel method with 4×4 μm scan size (a) AFM images of pentacene film on the nanostructured SiO₂ layer with 1×1 μm scan size (b).

**Table 1**
AFM data obtained from surface analysis of n-Si covered with/without the nanostructured dielectric film (SiO₂) and the organic semiconductor (pentacene) film.

<table>
<thead>
<tr>
<th>Film surface</th>
<th>Max height (nm)</th>
<th>Average height (nm)</th>
<th>Average surface roughness (nm)</th>
<th>Root-mean-square surface roughness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-Si/SiO₂ thermally oxidized (50 nm) film</td>
<td>2.13</td>
<td>1.22</td>
<td>0.26</td>
<td>0.31</td>
</tr>
<tr>
<td>n-Si/SiO₂ nanoparticle film</td>
<td>15.49</td>
<td>7.93</td>
<td>1.53</td>
<td>1.93</td>
</tr>
<tr>
<td>n-Si/SiO₂/pentacene film</td>
<td>65.09</td>
<td>26.66</td>
<td>5.23</td>
<td>7.14</td>
</tr>
</tbody>
</table>

**Fig. 3.** Plot of \( I_{ds} - V_{ds} \) under various gate voltages.

**Fig. 4.** Plot of \( \log I_{ds} - V_g \) under \( V_{ds} = 20 V \).
Vᵦ = 0. The photosensitivity of the studied transistor is also higher than that of polymer thin film transistors based on poly(2-methoxy-5-(2-ethyl-hexyloxy)-1,4-phenylene vinylene), a common conductive polymer used in OTFT technology [38]. This suggests that the photosensitivity behavior of the studied transistor depends on the photo properties of pentacene and nanostructure of SiO₂ dielectric layer. SiO₂ nanoparticles synthesized with sol–gel technique used in the gate insulating layer performs excellent light scattering behavior as a result of the increased surface area and finally to enhance photosensitivity due to the photocurrent created between source and drain of the pentacene OTFT.

For phototransistors, another important parameter is photosensitivity and it is expressed by the following relation [39]:

$$ R = \frac{I_{ph} (I_{ill} - I_{dark})}{P_{opt}} $$

where Iₚₜₕ is the drain source photocurrent, Pₚₜₒₜ is the incident optical power, P is the power of the incident light per unit area, Iₐᵦ is the drain source current under illumination, Iₐₖₐᵦ is the drain source current under dark and A is the effective device area. The R value for the transistor was found to be 100 mA/W. This value is several orders of magnitude higher than that reported (0.7 mA/W) for thin film organic polymer phototransistors [40,41].

From all the above, it is obvious that the morphology of the pentacene thin film (as it was deposited on the present nano-SiO₂ dielectric surface) was improved in relation to other structures proposed in literature. In combination with the light scattering properties due to nano-textured surfaces, our phototransistor with SiO₂ nanoparticle dielectric insulating layer exhibits improved photoelectrical characteristics.

4. Conclusions

The photosensing properties of the pentacene thin film transistor fabricated on n-Si substrate with nanostructured SiO₂ as gate dielectric have been investigated. The phototransistor shows p-channel characteristics. The photosensitivity (Iₚₜₕ/Iₐₖₐᵦ) of the transistor is 630.4 under 100 mW/cm² light illumination intensity at the off state. The nanosized SiO₂ particles synthesized with sol–gel technique used in the gate insulating layer performs excellent light scattering behavior as a result of increased surface area at the SiO₂ film to enhance photosensitivity due to the photocurrent created between source and drain of the pentacene OTFT. Besides the roughness of the SiO₂ and SiO₂/pentacene film was found to be small that is an important factor for the high electrical performance of the OTFT. The light scattering properties of the nanostructured film can be simply controlled over a wide range by simply varying the SiO₂ nanoparticle size. Finally, the field effect mobility of OTFT was found to be 2.96 cm²/V s.

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References