Microelectronic Engineering 87 (2010) 635–640

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

High-mobility pentacene phototransistor with nanostructured SiO_2 gate dielectric synthesized by sol–gel method

S. Okur [a,*], F. Yakuphanoglu [b], E. Stathatos [c]

[a] Department of Physics, Faculty of Science, İzmir Institute of Technology, Gülbahçe, Campus, Urla, İzmir 35430, Turkey
[b] Department of Physics, Faculty of Arts and Sciences, Firat University, Elazığ, Turkey
[c] Department of Electrical Engineering, Technological-Educational Institute of Patras, 263 34 Patras, Greece

ARTICLE INFO

Article history:
Received 17 May 2009
Received in revised form 30 July 2009
Accepted 28 August 2009
Available online 3 September 2009

Keywords:
Organic semiconductor
Pentacene
Phototransistor
Nanostructured SiO_2 insulating gate
Sol–gel method
Thin film phototransistor
Interface state density

ABSTRACT

We have fabricated a pentacene based phototransistor by employing a modified nanostructured SiO_2 gate dielectric. The photosensing properties of the pentacene thin film transistor fabricated on n-Si substrate with nanostructured SiO_2 as gate dielectric have been investigated. The photocurrent of the transistor increases with an increase in illumination intensity. This suggests that the pentacene thin film transistor behaves as a phototransistor with p-channel characteristics. The photosensitivity and responsivity values of the transistor are 630.4 and 0.10 A/W, respectively at the off state under AM 1.5 light illumination. The field effect mobility of the pentacene phototransistor was also found to be 2.96 cm^2/Vs. The nanostructured surface of the gate possibly is the cause of the high-mobility value of the phototransistor due to light scattering from the increased surface area.

1. Introduction

Sputtering and thermal chemical vapor deposition (CVD), are common techniques to create a smooth insulating gate films for normal organic and inorganic field-effect transistors. Light-trapping plays a key role for crystalline Si thin film solar cells and phototransistors. The application of textured glass substrates instead of planar glass substrates is an attractive way to implement light trapping [1,2]. Several techniques are used to fabricate textured rough surface on transparent conductive oxide (TCO) glasses for solar cell applications. A simple chemical etching step in diluted acid, yields a textured surface which can be adjusted to give optimal light scattering over a wide wavelength range. Rech et al. showed that ZnO:Al films prepared by magnetron sputtering and post deposition wet chemical etching demonstrate an effective light trapping and the textured surface reduces reflection losses at the ZnO:Al/Si-interface with excellent light scattering properties for silicon thin film solar cells and modules [3,4]. Grained polycrystalline silicon (poly-Si) films were prepared on nano-textured glass substrates by epitaxial thickening of seed layers formed by the aluminum-induced layer exchange (ALILE) process [5,6] for poly-Si thin film solar cell application with 8% efficiencies with improved material quality [7–10].

The insulating film which plays the role of the gate in a phototransistor needs to combine high capacitance for low level leakage and an adequate surface texture to introduce light scattering and subsequent light trapping to increase photo sensitivity by increasing the number of excited photo carriers. For efficient light trapping, the substrate textures should be in the order of the incoming light wavelength.

The sol–gel method for the synthesis of inorganic nanoparticles such as ZnO, TiO_2 and SiO_2 [11–15] has become one of the most popular chemical procedures. The reason of this popularity stems from the fact that sol–gel synthesis is easy and it is carried out at ambient or slightly elevated temperature. Indeed, the sol–gel method has led to the synthesis of a great variety of materials, the range of which is continuously expanding. A typical sol–gel route for making silicon oxide matrices and thin films is followed by hydrolysis of alkoxides, for example, alkoxysilanes. However, a review of the recent literature reveals an increasing interest in another sol–gel route based on organic acid solvolysis of alkoxides [16–18]. As it has been earlier found by Pope and Mackenzie [19] and later verified by others [20], organic (for example, acetic) acid solvolysis proceeds by a two step mechanism which involves intermediate ester formation. Simplified reaction schemes showing gel formation either by hydrolysis or organic acid solvolysis are

* Corresponding author. Tel.: +90 2327507706; fax: +90 2327507707.
E-mail address: salihokur@iyte.edu.tr (S. Okur).

0167-9317/$ - see front matter
doi:10.1016/j.mee.2009.08.029

presented by the following reactions. (in the following reactions only one of the four alkoxy groups is taken into account for reasons of simplicity, while acetic acid (AcOH) is chosen to represent organic acids in organic acid solvolysis):

$$\text{Hydrolysis}\quad \text{Si—OR} + H_2O \rightarrow \text{Si—OH} + \text{ROH} \tag{1}$$

$$\text{Acetic acid solvolysis}\quad \text{Si—OR} + \text{AcOH} \rightarrow \text{Si—OAc} + \text{ROH} \tag{2a}$$

$$\text{ROH} + \text{AcOH} \rightarrow \text{ROAc} + H_2O \tag{2b}$$

$$\text{Si—OAc} + \text{ROH} \rightarrow \text{ROAc} + \text{SiOH} \tag{2c}$$

$$\text{Si—OR} + \text{Si—OAc} \rightarrow \text{ROAc} + \text{Si—O—Si} \tag{2d}$$

R is a short alkyl chain (for example, methyl, ethyl or isopropyl). Hydrolysis (1) produces highly reactive hydroxide species Si–OH, which, by inorganic polymerization, produce oxide, i.e. Si–O–Si that is the end product of the sol–gel process. More complicated is acetic acid solvolysis (2) where several different possibilities may define different intermediate routes to obtain oxide. Reaction (2a) is a prerequisite of the remaining three reactions. Occurrence of reaction (2b) would mean that gel formation would proceed by an intermediate hydrolysis caused by water created through (2b). Reaction (2c) would create highly reactive Si–OH which would form oxide, while reaction (2d) directly leads to oxide formation. The sol–gel precursor used in the present work is not a simple alkoxide but a hybrid precursor that consists of a polyether chain with two triethoxysilane end groups covalently bound by urea bridges (ureasil), as can be seen in Scheme 1. This material was used because it helps to make very uniform nanocrystalline films on silicon wafers even after calcinations at high temperature to remove any of the organic material producing pure SiO_2 which was finally the insulating material for the gate of the phototransistor.

Besides, optical response of pentacene in the UV and visible region is promising for use in phototransistor applications [21,22]. Combination of light detection and signal amplification in a single device without any noise problems [23–25] gives superior performance to pentacene based organic thin film transistors (OTFTs) for photo sensor applications [26]. As a consequence, organic field-effect phototransistors play an interesting role in the electronic devices technology, since they can be used for light induced switches, light triggered amplification, detection circuits and, in photOFET arrays for highly sensitive image sensors [27].

In this work, we present the fabrication of a high-mobility pentacene phototransistor (2.96 cm^2/Vs), employing nanostructured SiO_2 gate dielectric which was synthesized by sol–gel method, to investigate the photosensing characteristics of the device under visible light illumination.

2. Experimental

A top contact thin film transistor (OTFT) has been fabricated with a p-channel organic semiconductor pentacene with 98% purity, purchased from Sigma–Aldrich. An n-type (N/Phos) single crystal silicon wafer pre-polished on one side with <1 0 0> surface orientation, thickness of 530 μm, diameter of 100 mm and 2.00 Ω cm resistivity was purchased from Si-Mat Silicon Wafers Company, and used as a substrate. The Si-wafer was covered with a thin SiO_2 layer with thickness 200 nm which was prepared by the sol–gel technique. All chemicals used in the sol–gel method have been purchased from Aldrich.

The hybrid organic/inorganic precursor used in the preparation of SiO_2 thin films is presented in Scheme 1 and it was synthesized as following: Two different unhydrolyzed alkoxysilane-polyether precursors were prepared as in previous publications [18,27].

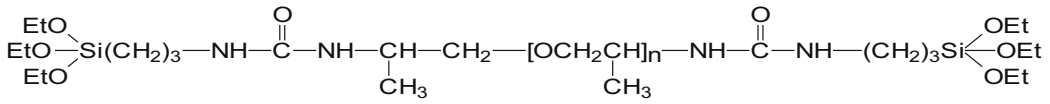
Poly(propylene glycol)bis(2-aminopropylether) of molecular weight 230 and 3-isocyanatopropyltriethoxysilane (ICS) (molar ratio [ICS]/[diamine]=2) were mixed in tetrahydrofuran (THF) under reflux (64 °C) for 6 h. The isocyanate group of ICS reacts with the amino groups of poly(propylene glycol)bis(2-aminopropylether) (acylation reaction) producing urea connecting groups between the polymer units and the inorganic part. After evaporation of THF under vacuum, a viscous precursor was obtained, which is stable at room temperature for several months. The abbreviated name of the thus prepared precursor used in the present work is ICS-PPG230.

2.1. Sol–gel synthesis and film deposition

Two grams of the ICS-PPG230 precursor was mixed with 2 g of ethanol. After stirring for 5 min, acetic acid (AcOH) was added and the mixture was stirred for about 5 h. Finally, thin films of composite organic–inorganic materials were formed on silicon wafers of desired size with spin-coating technique at a speed of 3000 rpm. The Si substrates were previously cleaned with sonication consecutively in a bath of ethanol and acetone. A thin and optically uniform film of SiO_2 was obtained after calcination at 500 °C in a furnace, suggested that all organic content was eliminated. The furnace temperature was incremented at a ramp rate of 15 °C min^{-1}; this temperature was held for 15 min and then silicon wafers were cooled to room temperature. The film thickness of SiO_2 film was approximately 200 nm according to SEM cross-sectional images.

A 200 nm thick pentacene film was deposited on the SiO_2 layer under vacuum after thermal evaporation and it was used as the active layer in the organic thin film transistor. A gold thin film (purity, 99.95%) with a thickness of 200 nm was thermally evaporated from a tungsten filament under 6×10^{-6} Torr vacuum. Gold top contacts on the n-Si/SiO_2/pentacene structure were formed having a channel length of 30 μm and channel width of 300 μm using a shadow mask. The schematic structure of n-Si/nano-SiO_2/pentacene/Au OTFT device is shown in Fig. 1. The current–voltage characteristics (I_{ds}–V_{ds} and I_{ds}–V_{gs}) of the OTFT were measured with a KEITHLEY 2400 Source meter and a KEITHLEY 6517 Electrometer. Photovoltaic measurements were employed using a 200 W halogen lamp.

The morphology of the pentacene thin film as deposited on the nano-SiO_2 dielectric surface was examined with a Solver P47H Atomic Force Microscope (NT-MTD) operating in tapping mode in air at room temperature. Diamond-like carbon (DLC) coated NSG01-DLC silicon cantilevers (from NT-MTD) with a 2 nm tip apex curvature were used at its resonance frequency of 150 kHz.



Scheme 1. Chemical structure of ureasil precursor (ICS-PPG230 and $n \sim 3$).

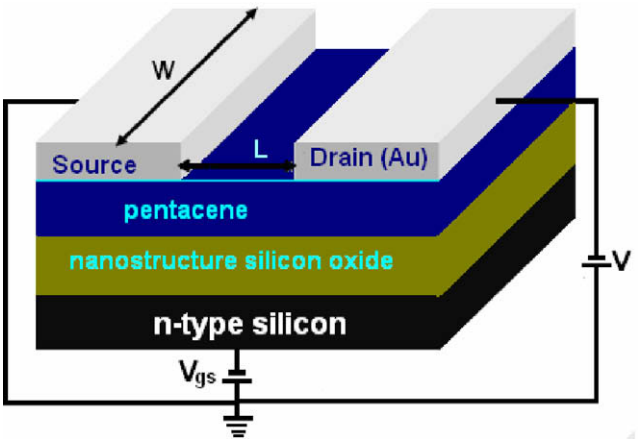


Fig. 1. Schematic structure of n-Si/nano-SiO_2/pentacene/Au OTFT device.

The Nova 914 software package was used to control the SPM system and for the analysis of the AFM images.

3. Results and discussion

In order to improve the working properties of pentacene thin film transistor, we modified the surface properties of the SiO_2 dielectric layer using SiO_2 nanoparticles formed by sol–gel fabrication technique. For the surface morphology of the dielectric layer, the two-dimensional and three-dimensional atomic force microscopy (AFM) images of SiO_2 dielectric surface formed with sol–gel method and pentacene film deposited on the SiO_2 were obtained by AFM as they are shown in Fig. 2a and b. The AFM image shows a homogeneous pentacene film surface with the root-mean-square (rms) roughness of 7.5 nm. As seen from Fig. 2a, the pentacene grains on SiO_2 form ellipsoidal particle shapes with aspect ratio of 70 nm/90 nm. The grain size may be attributed to the wetting properties of the dielectric layer. The surface roughness of the SiO_2 gate dielectric have an important effect on the performance of the organic phototransistor, since the charge carrier transport in the active layer is affected by the dielectric layer morphology due to light scattering mechanism. Table 1 shows the AFM data obtained from the surface analysis of n-Si covered with/without the nanostructured dielectric film (SiO_2) and the organic semiconductor (pentacene) film. The surface roughness of nanostructured SiO_2 surface on n-Si substrate has relatively increased compared to thermally oxidized SiO_2 surface. Hence, the light scattering and trapping inside the nanostructured gate are improved. This might be one of the reasons for higher photocurrent and mobility value for pentacene OTFT with a nanostructured SiO_2insulating gate.

The drain current–voltage characteristics of the pentacene thin film transistor under different gate voltages are shown in Fig. 3. As seen in Fig. 3, the drain source current of the transistor increases with negative gate voltages. This suggests that the thin film transistor indicates a clear p-channel transistor behavior. At lower voltages, the drain current–voltage curves exhibit good linearity of response. This confirms that a good ohmic contact was established between the pentacene and gold contacts.

The drain current in the linear region can be expressed by:

$$I_{ds} = \frac{W}{L}\mu C_i\left[(V_g - V_{th})V_d - \frac{V_d^2}{2}\right] \quad (3)$$

where I_{ds} is the drain source current, W is the width of channel, L is the channel length, C_i is the capacitance of the oxide layer, V_g is the gate voltage, μ is the mobility and V_{th} is the threshold voltage [28].

On the other hand, the drain current in the saturation region can be expressed by: [28]

$$I_{ds} = \frac{W}{2L}\mu C_i(V_G - V_{th})^2 \quad (4)$$

The oxide layer capacitance for the transistor was determined from capacitance–voltage curve under 100 kHz and was found to be 7.45 nF/cm^2. The field effect mobility and threshold voltage of OTFT from $I_{ds}^{1/2}$–V_g plot were found to be 2.96 cm^2/Vs and 3.4 V, respectively.

With the presence of nanostructured SiO_2, the mobility of pentacene OTFT was reached to be 2.96 cm^2/Vs. Therefore, pentacene based OTFT performance is determined by the quality of SiO_2 layer. The mobility of the studied transistor is higher than that of another transistor structured also with pentacene [29]. We evaluated that the nanostructure of SiO_2 gate dielectric contributes to the high performance of pentacene field-effect transistor. The higher mobility of the transistor can be attributed to the morphology of pentacene film on the nanostructured gate material and the dielectric/surface properties of transistor. As seen in AFM images, the transistor in our studies appears a relatively smooth surface with small roughness. This suggests that the mobility is improved by surface roughness elimination. The effective mobility in polycrystalline materials depends on phonon scattering, impurity scattering, interface roughness scattering, defect scattering, and grain boundary scattering mechanisms [30,31]. The roughness of the studied transistor is lower than that of pentacene phototransistors referred in literature [29,32] and thus, the higher mobility of the transistor depends on the surface roughness of the SiO_2, as the mobility is improved by reduction in surface scattering mechanisms taken place in the presence of a smoother interface.

The threshold voltage for the transistor can be defined as follows [33–35],

$$V_{th} = \frac{qn_o d}{C_i} \quad (5)$$

where q is the electronic charge, n_o is the density of majority carriers and d is the thickness of the organic semiconductor. The density of majority carriers for the transistor was determined using Eq. (3) and was found to be 1.64×10^{16} cm^{-3}.

The inverse sub-threshold slope for the transistor is expressed as follows: [35],

$$S = \left[\frac{d\log(I_d)}{dV_g}\right]^{-1} \quad (6)$$

The S value for the transistor was determined from Fig. 4 and was found to be 3.98 V/dec. This value is a measure of the turn-on speed of the transistor and it indicates the presence of trap behavior and interface quality between the dielectric and active layer [35]. The S value of the present transistor is higher than that pentacene transistor proposed in literature [29]. We finally evaluate that the studied transistor give a higher mobility with a smaller S value, which exhibits better performance.

$$D_{it} = \left[\frac{S\log(e)}{kT/q} - 1\right]\frac{C_i}{q} \quad (7)$$

The interface trap density for the transistor can be calculated by the following relation [36,37]:
where k is the Boltzmann constant, T is the temperature, q is the electronic charge and C_i is 7.45 nF/cm^2. With C_i and S values, the D_{it} was calculated to be 3.02×10^{12} cm^{-2} eV^{-1}. The D_{it} value of the studied transistor is in agreement with that obtained for another pentacene transistor [29]. Fig. 5 shows the drain current curves of the pentacene thin film transistor under various illumination conditions. As seen in Fig. 5, the drain–source current of

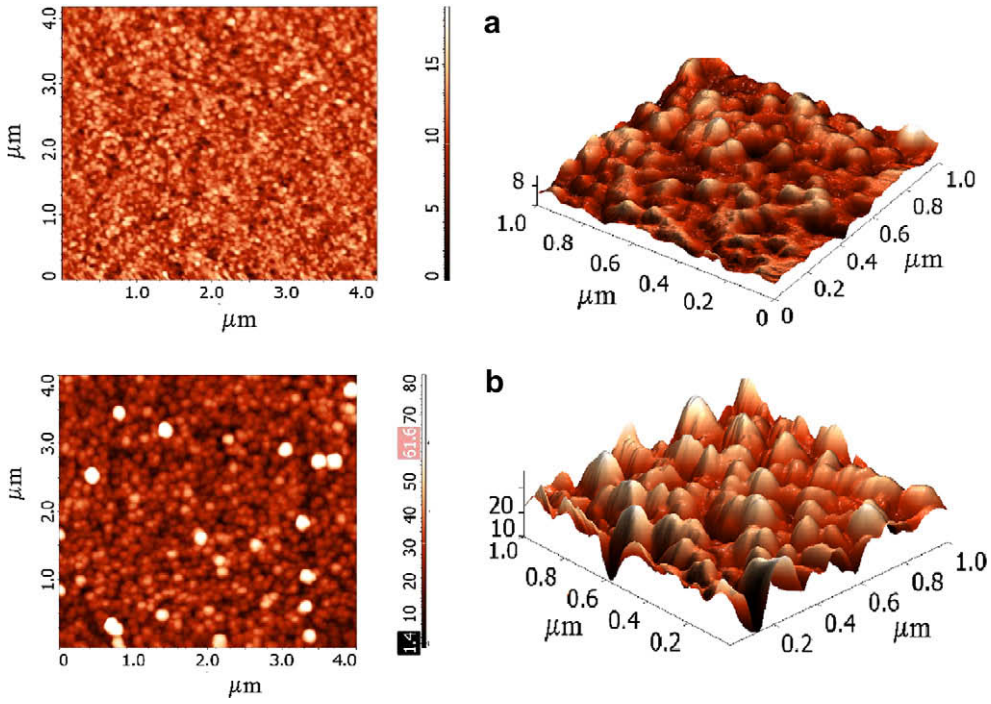


Fig. 2. Atomic force microscopy (AFM) images of SiO_2 dielectric surface formed with the sol–gel method with 4×4 μm scan size (a) AFM images of pentacene film on the nanostructured SiO_2 layer with 1×1 μm scan size (b).

Table 1
AFM data obtained from surface analysis of n-Si covered with/without the nanostructured dielectric film (SiO_2) and the organic semiconductor (pentacene) film.

Film surface	Max height (nm)	Average height (nm)	Average surface roughness (nm)	Root-mean-square surface roughness (nm)
n-Si/SiO_2 thermally oxidized (50 nm) film	2.13	1.22	0.26	0.31
n-Si/SiO_2 nanoparticle film	15.49	7.93	1.53	1.93
n-Si/SiO_2/ pentacene film	65.09	26.66	5.23	7.14

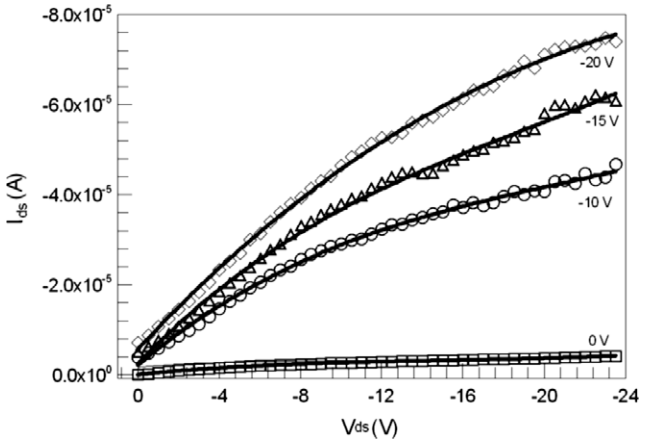


Fig. 3. Plot of I_{ds}–V_{ds} under various gate voltages.

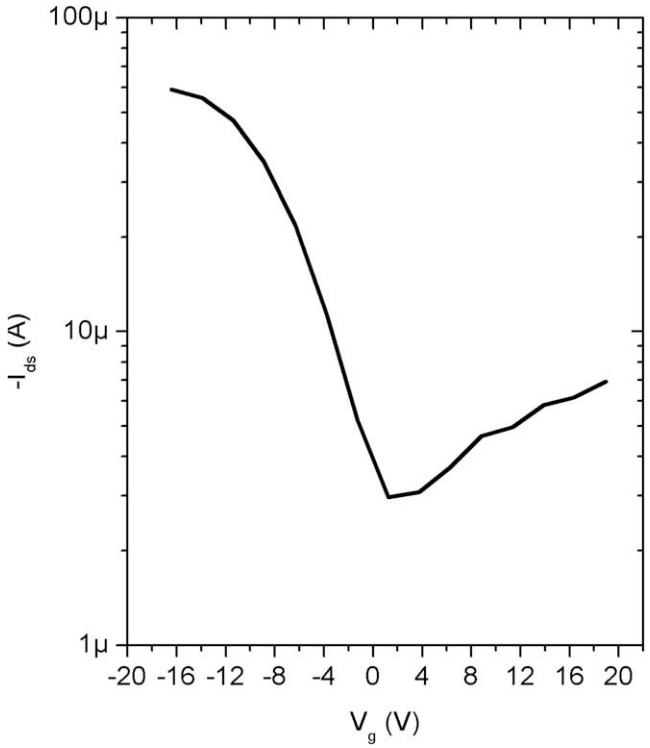


Fig. 4. Plot of log I_{ds}–V_g under $V_{ds} = -20$ V.

the transistor increases with illumination due to the flow of mobile carriers in the channel layer of the transistor via source–drain voltage. This confirms that the pentacene thin film transistor is a phototransistor. The photosensitivity (I_{ph}/I_{dark}) at 29 V was measured as 630.4 at an illumination intensity of 100 mW/cm^2 under

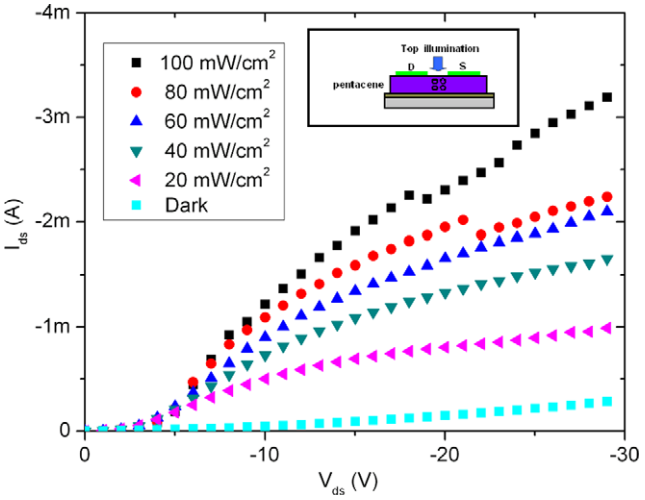


Fig. 5. Plot of I_{ds}–V_{ds} under various illumination light intensities.

$V_g = 0$. The photosensitivity of the studied transistor is also higher than that of polymer thin film transistors based on poly(2-methoxy-5-(2′-ethyl-hexyloxy)-1,4-phenylene vinylene), a common conductive polymer used in OTFT technology [38]. This suggests that the photosensing behavior of the studied transistor depends on the photo properties of pentacene and nanostructure of SiO_2 dielectric layer. SiO_2 nanoparticles synthesized with sol–gel technique used in the gate insulating layer performs excellent light scattering behavior as a result of the increased surface area and finally to enhance photosensitivity due to the photocurrent created between source and drain of the pentacene OTFT.

For phototransistors, another important parameter is photoresponsivity and it is expressed by the following relation [39]:

$$R = \frac{I_{ph}}{P_{opt}} \frac{(I_{ill} - I_{dark})}{P \cdot A} \quad (8)$$

where I_{ph} is the drain source photocurrent, P_{opt} is the incident optical power, P is the power of the incident light per unit area, I_{ill} is the drain source current under illumination, I_{dark} is the drain source current under dark and A is the effective device area. The R value for the transistor was found to be 100 mA/W. This value is several orders of magnitude higher than that reported (0.7 mA/W) for thin film organic polymer phototransistors [40,41].

From all the above, it is obvious that the morphology of the pentacene thin film (as it was deposited on the present nano-SiO_2 dielectric surface) was improved in relation to other structures proposed in literature. In combination with the light scattering properties due to nano-textured surfaces, our phototransistor with SiO_2 nanoparticle dielectric insulating layer exhibits improved photoelectrical characteristics.

4. Conclusions

The photosensing properties of the pentacene thin film transistor fabricated on n-Si substrate with nanostructured SiO_2 as gate dielectric have been investigated. The phototransistor shows p-channel characteristics. The photosensitivity (I_{ph}/I_{dark}) of the transistor is 630.4 under 100 mW/cm^2 light illumination intensity at the off state. The nanosized SiO_2 particles synthesized with sol–gel technique used in the gate insulating layer performs excellent light scattering behavior as a result of increased surface area at the SiO_2 film to enhance photosensitivity due to the photocurrent created between source and drain of the pentacene OTFT. Besides the roughness of the SiO_2 and SiO_2/pentacene film was found to be small that is an important factor for the high electrical performance of the OTFT. The light scattering properties of the nanostructured film can be simply controlled over a wide range by simply varying the SiO_2 nanoparticle size. Finally, the field effect mobility of OTFT was found to be 2.96 cm^2/V s.

Acknowledgment

This study was financially supported with grants of major research projects, DPT2003K120390 by Turkish State Planning Organization (DPT).

References

[1] N.-P. Harder, D. Le Bellac, E. Royer, B. Rech, G. Schöpe, J. Müller, in: Proceedings of the Nineteenth European Photovoltaic Solar Energy Conference, Paris, France, 2004, p. 1355.
[2] C. Gandon, C. Marzolin, B. Rogier, E. Royer, Patent WO 02/02472 A1, 2002.
[3] O. Kluth, B. Rech, L. Houben, S. Wieder, G. Schope, C. Beneking, H. Wagner, A. Loffl, H.W. Schock, Thin Solid Films 351 (1999) 247.
[4] B. Rech, O. Kluth, T. Repmann, T. Roschek, J. Springer, J. Muller, F. Finger, H. Stiebig, H. Wagner, Sol. Energy Mater. Sol. Cells 74 (2002) 439.
[5] O. Nast, T. Puzzer, L.M. Koschier, A.B. Sproul, S.R. Wenham, Appl. Phys. Lett. 73 (1998) 3214.
[6] B. Rau, I. Sieber, J. Schneider, M. Muske, M. Stöger-Pollach, P. Schattschneider, S. Gall, W. Fuhs, J. Cryst. Growth 270 (2004) 396.
[7] P. Widenborg, A. Straub, A.G. Aberle, J. Cryst. Growth 276 (2005) 19.
[8] I. Gordon, L. Carnel, D. Van Gestel, G. Beaucarne, J. Poortmans, Prog. Photovoltaics: Res. Appl. 15 (2007) 575.
[9] (a) F. Finger, R. Carius, T. Dylla, S. Klein, S. Okur, M. Günes, J. Optoelectron. Adv. Mater. 7 (2005) 83;
(b) M. Egilmez, A. Gunel, S. Okur, M. Tanoglu, L. Ozyuzer, Key Eng. Mater. 266 (2004) 1197.
[10] S. Okur, M. Güneş, O. Göktaş, F. Finger, R. Carius, J. Mater. Sci. – Mater. Electron. 15 (2004) 187.
[11] V. Khrenov, M. Klapper, M. Koch, K. Mullen, Macromol. Chem. Phys. 206 (2005) 95.
[12] I.A. Toutorski, T.E. Tkachenko, B.V. Pokidko, J. Sol–Gel Sci. Technol. 26 (2003) 505.
[13] Katsuhiko Ariga 1, Yuri Lvov, Izumi Ichinose, Toyoki Kunitake, Appl. Clay Sci. 15 (1999) 137.
[14] T. Moritz, J. Reiss, K. Diesner, D. Su, A. Chemseddine, J. Phys. Chem. B 101 (1997) 8052.
[15] T. Schmidt, G. Müller, L. Spanhel, K. Kerkel, A. Forchel, Chem. Mater. 10 (1998) 65.
[16] H.W. Green, P.K. Le, J. Grey, T.T. Au, M.J. Sailor, Science 276 (1997) 1826.
[17] E. Stathatos, P. Lianos, U. Lavrencic-Stangar, B. Orel, Adv. Mater. 14 (2002) 354.
[18] E. Stathatos, P. Lianos, B. Orel, A. Surca Vuk, R. Jese, Langmuir 19 (2003) 7587.
[19] E.J.A. Pope, J.D. Mackenzie, J. Non-Cryst. Solids 87 (1986) 185.
[20] (a) D.P.J. Birnie, Mater. Sci. 3 (2000) 367;
(b) S. Okur, John F. Zasadzinski, J. Appl. Phys. 85 (1999) 756.
[21] Y.Y. Noh, D.Y. Kim, K. Yase, J. Appl. Phys. 98 (2005) 074505.
[22] M. Debucquoy, S. Verlaak, S. Steudel, K. Myny, J. Genoe, P. Heremans, Appl. Phys. Lett. 91 (2007) 103508.
[23] A.J. Seeds, A.A.A. Salles, IEEE Trans. Microwave Theory Tech. 38 (1990) 577.
[24] A. Madjar, P.R. Herczfeld, A. Paolella, IEEE Trans. Microwave Theory Tech. 40 (1992) 1681.
[25] M.A. Romeo, M.A.G. Martinez, P.R. Herczfeld, IEEE Trans. Microwave Theory Tech. 44 (1996) 2279.
[26] B. Lucas, A. El Amrani, A. Moliton, Mol. Cryst. Liq. Cryst. 485 (2008) 955.
[27] E. Stathatos, P. Lianos, U. Lavrencic-Stangar, B. Orel, P. Judeinstein, Langmuir 16 (2000) 8672.
[28] N. Marjanovic, Th.B. Singh, G. Dennler, S. Güneş, H. Neugebauer, N.S. Sariciftci, R. Schwödiauer, S. Bauer, Org. Electron. 7 (2006) 188.
[29] R.F. Pierret, Semiconductor Device Fundamentals, Addison-Wesley Publishing Company, 1996.
[30] S.M. Sze, Physics of Semiconductor Devices, second ed., John Wiley and Sons, 1981.
[31] H.-S. Seo, Y.-S. Jang, Y. Zhang, P. Syed Abthagir, J.H. Choi, Org. Electron. 9 (2008) 432.
[32] J.W. Orton, M.J. Powell, Rep. Prog. Phys. 43 (1980) 1263.
[33] S.S. Ahmed, D.M. Kim, H. Shichijo, IEEE Electron Device Lett. 6 (1985) 313.
[34] S. Okur, F. Yakuphanoglu, Sensor. Actuat. A 149 (2009) 241.
[35] L.A. Majewski, M. Grell, Synthetic Met. 151 (2005) 175.
[36] G. Horowitz, Adv. Funct. Mater. 13 (2003) 53.
[37] R.N. Christopher, C.D. Frisbie, D.A. da Silva Filho, J.L. Bredas, C.E. Paul, R.M. Kent, Chem. Mater. 16 (2004) 4436.

[38] J.H. Seo, J.-H. Kwon, S.-I. Shin, K.-S. Suh, B.-K. Ju, Semicond. Sci. Technol. 22 (2007) 1039.
[39] K.N.N. Unni, D.S. Sylvie, J.M. Nunzi, J. Phys. D: Appl. Phys. 38 (2005) 1148.
[40] Y.R. Liu, J.B. Peng, P.T. Lai, Thin Solid Films 516 (2008) 4295.
[41] M.C. Hamilton, S. Martin, J. Kanicki, IEEE Trans. Electron Dev. 51 (2004) 877.