FABRICATION AND CHARACTERIZATION OF SOI BASED PHOTODETECTORS WITH GRAPHENE ELECTRODE

A Thesis Submitted to
the Graduate School of Engineering and Sciences of
İzmir Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of

DOCTOR OF PHILOSOPHY

in Photonics Science and Engineering

by
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July 2023
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ACKNOWLEDGMENTS

I would like to express my gratitude to my supervisor Prof. Dr. Cem Çelebi for his continuous guidance and support throughout my PhD. I thank him for providing an opportunity to access of all the facilities of the QDL. Therefore, I am very grateful for his invaluable help, guidance and his endless patience as well as his understanding provided during this thesis. Working with him has been a pleasure and privilege for me.

I would like to thank my committee members of my thesis Prof. Dr. Canan Varlıklı, Assoc. Prof. Dr. Serkan Ateş, Prof. Dr. Ceylan Zafer and Prof. Dr. Aytaç Gürhan Gökçe for their participations. I am also thankful to Assist. Prof. Dr. Özhan Ünverdi for his motivation and great contributions to this thesis.

I am also grateful to Dr. Mehmet Fidan and Dr. Hasan Aydın for all brainstorming and help and all the members of QDL for their support and friendly work environment. In addition, I would like to thank the researchers in Katip Çelebi University Central Research Laboratory for Raman spectroscopy measurements and give my dearest thanks to all of my colleagues at Semiconductor Devices Development Unit in Ermaksan Optoelectronic R&D Center who helped me through my thesis with their collaborations in device fabrication and surface characterization processes and gave me motivation with their kind friendships. I am also thankful to “fresh” Dr. Dilce Özkendir İnanç who always supported and encouraged me through this whole process during the time since undergraduate.

In addition, I would like to acknowledge my institution, İzmir Institute of Technology, for providing me research facilities in Center for Materials Research of İzmir Institute of Technology (İYTE MAM) during my PhD study. Finally, I want to deeply thank to my parents for leading me to this stage and their supports and love up to today. Also, I would like to express my heart-felt gratitude to Dilek Kuyucu for ceaseless support.

This work is supported within the scope of the scientific research project as a part of the Project No. BAP113 which was accepted by the Yaşar University Project Evaluation Commission (PEC) and YÖK 100/2000 PhD program on sensor technologies.

Last but not least, I want to thank me for believing in me. I want to thank me for doing all this hard work and never quitting.

ABSTRACT

FABRICATION AND CHARACTERIZATION OF SOI BASED PHOTODETECTORS WITH GRAPHENE ELECTRODE

This thesis presents the pioneering methods for the design, fabrication process, and performance evaluation of graphene (G) and n-type silicon (n-Si) based self-powered one dimensional (1D) and two dimensional (2D) photodetector arrays (PDAs) on a silicon on insulator (SOI) substrate. In the device structure, monolayer G is utilized as hole collecting transparent conductive electrode (TCE) and n-Si is used as light absorbing material, respectively. After analyzing the photo-response characteristics of single pixel G/n-Si diode on SOI, we fabricated G/n-Si based Schottky barrier 1D PDAs with *common* G electrode, *separate* G electrode and 2D PDA with individual G electrodes on linearly arrayed n-Si channels, respectively. Each G/n-Si diodes exhibited a clear rectifying Schottky character with low dark current and diode parameters were analyzed using the current-voltage measurement. Besides, all diodes demonstrated a clear photovoltaic activity under the light illumination and maximum responsivity at 660 nm peak wavelength.

Each diode in PDA revealed similar device performances under self-powered mode in terms of an I_{light}/I_{dark} ratio up to 10^4, a responsivity of ~0.1 A/W and a response speed of ~1.3 μs at 660 nm wavelength. The optical crosstalk was extremely low between neighboring diodes and also it could be greatly minimized when G is used as separated electrode on arrayed Si up to ~0.10% (-60 dB) per array. Time dependent photocurrent spectroscopy measurements revealed an excellent photocurrent reversibility of both device types. In the diode structure, the homogeneity of the graphene film transferred on n-Si were examined by Raman mapping and correlated with the sensitivity of diode to incoming light. This thesis paves the way for the new generation of optoelectronic devices with various potential by integrating G and SOI technology to PDA devices with ease of fabrication.

ÖZET

GRAFEN ELEKTROTLU SOI TABANLI FOTODEDEKTÖRLERİN ÜRETİMİ VE KARAKTERİZASYONU

Bu tez, yalıtımlı Si (SOI) alttaş üzerinde grafen (G) ve n-tipi silikon (n-Si) tabanlı kendi kendine çalışan bir boyutlu (1D) ve iki boyutlu (2D) fotodedektör dizilerinin (PDAs) tasarımı, üretim süreci ve performans değerlendirmesi için öncü yöntemler sunmaktadır. Aygıt yapısında sırasıyla tek tabakalı G, deşik toplayıcı saydam iletken elektrot olarak (TCE) ve n-Si ise ışığı soğuran malzeme olarak kullanılmaktadır. SOI üzerinde tek piksel G/n-Si diyotunun foto-tepki özelliklerini analiz ettikten sonra, sırasıyla *ortak* ve *ayrı* G elektrotlu G/n-Si tabanlı Schottky bariyer 1D PDA'lar ve doğrusal olarak dizilmiş n-Si kanalları üzerinde ayrı G elektrotlu 2D PDA'lar ürettik. Her bir G/n-Si diyot, düşük karanlık akım ile belirgin bir doğrultucu Schottky karakteri sergilemiştir ve diyot parametreleri, akım-voltaj ölçümü kullanılarak analiz edilmiştir. Ayrıca, tüm diyotlar, ışık aydınlatması altında net bir fotovoltaik aktivite ve 660 nm tepe dalga boyunda maksimum tepki göstermiştir.

PDA'daki her bir diyot, 660 nm dalga boyunda kendi gücünü sağlayan mod altında, 10^4 'e kadar I_{light}/I_{dark} oranı, ~0,1 A/W duyarlılık ve ~1,3 μs yanıt hızı açısından benzer aygıt performansları ortaya koymuştur. Optik karışma, komşu diyotlar arasında son derece düşüktür ve ayrıca G, dizili Si üzerinde ayrı elektrot olarak kullanıldığında, dizi başına ~%0,10 'a (-60 dB) kadar büyük ölçüde minimize edilmiştir. Zamana bağımlı foto-akım ölçümleri, her üç aygıt tipinin de ürettiği fotoakımın kendini mükemmel bir şekilde yenileyebildiğini ortaya çıkarmıştır. Diyot yapısındaki n-Si üzerine transfer edilen grafen filmin homojenliği Raman haritalaması ile incelenmiştir ve diyotun gelen ışığa duyarlılığı ile ilişkilendirilmiştir. Bu tez, G ve SOI teknolojisini üretim kolaylığı ile PDA aygıtlara uyarlayarak çeşitli potansiyellere sahip yeni nesil optoelektronik aygıtlara zemin hazırlamaktadır.

To my Family

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LIST OF SYMBOLS

χ	Electron affinity
λ	Wavelength
μ	Mobility
ε_0	Vacuum permittivity
Φ_0	Neutral energy level
Φ_B	Schottky barrier height
Φ_G	Work function of graphene
Φ_{bi}	Built-in potential
Φ_m	Work function of metal
ε_s	Permittivity of semiconductor medium
Φ_{sc}	Work function of semiconductor
A^*	Richardson constant
B_w	Bandwidth
D^*	Specific detectivity
E_C^{sc}	Conduction band of semiconductor
E_F	Fermi level
E_F^m	Fermi level of metal
E_F^{sc}	Fermi level of semiconductor
E_V^{sc}	Valance band of semiconductor
E_g	Band gap energy
I_0	Saturation current
I_d	Dark current
I_p	Photocurrent
I_{sc}	Short-circuit current
J_s	Saturation current density
J_{sm}	Current density flowing from semiconductor into metal
R_s	Sheet resistance
V_0	Zero bias voltage
V_F	Forward bias voltage

V_R	Reverse bias voltage
V_b	Bias voltage
V_{oc}	Open-circuit voltage
W_d	Depletion region
k_B	Boltzmann constant
m^*	Effective mass
t_d	Decay time
t_r	Rise time
υ_f	Fermi velocity
Au	Gold
Cr	Chromium
Cu	Copper
$FeCl_3$	Iron (III) chloride
h	Planck constant
HCl	Hydrochloric acid
HF	Hydrofluoric acid
ITO	Indium Tin Oxide
ɳ	Ideality factor
N_d	Donor concentration
Ni	Nickel
SF_6	Sulfur hexafluoride
SiC	Silicon Carbide
SiO	Silicon monoxide
X_d	Depletion region width
A	Active junction area
E	Electric field
P	Light power
R	Responsivity
T	Absolute temperature
c	Speed of light
n	Carrier density
q	Elementary charge

LIST OF ABBREVIATIONS

1D	One-dimensional
2D	Two-dimensional
APCVD	Atmospheric Pressure Chemical Vapor Deposition
BESOI	Etch-back SOI
BOX	Buried oxide
BZ	Brillouin zone
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical vapor deposition
D^*	Specific detectivity
e-h	Electron - Hole
FE	Field Emission
FIR	Far-infrared
FWHM	Full Width Half Maximum
G	Graphene
G/n-Sc	Graphene/n-type semiconductor
GSi	Graphene/n-type silicon
GSOI	Graphene/Silicon-on-insulator
HOPG	Highly Ordered Pyrolytic Graphite
ILPP	Interdigitated lateral p-i-n photodetector
IPA	Isopropyl alcohol
ITO	Indium tin oxide
I-V	Current - Voltage
LED	Light emitting diode
MEMS	Microelectromechanical systems
MGM	Metal-Graphene-Metal
MIR	Mid-infrared
MS	Metal / Semiconductor
NEP	Noise-equivalent power
NIR	Near-infrared
n-Sc	n-type Semiconductor

n-Si	n-type Silicon
OLEDs	Organic light emitting diodes
PCB	Printed Circuit Board
PD	Photodetector
PDA	Photodetector array
PR	Photoresist
R.T.	Room Temperature
RIE	Reactive Ion Etching
SBH	Schottky Barrier Height
Sc	Semiconductor
SEM	Scanning electron microscope
SiC	Silicon Carbide
SIMOX	Separation by Implantation of Oxygen
SOI	Silicon-on-insulator
SOS	Silicon-on-sapphire
SRH	Shockley-Read-Hall
TCE	Transparent conductive electrode
TE	Thermal Emission
TFE	Thermionic Field Emission
TFT	Thin film transistor
THz	Terahertz
UHV	Ultra-High Vacuum
UV	Ultraviolet

CHAPTER 1

INTRODUCTION

The conversion of light into electrical signal or vice-versa is the indisputable significance for today's technologies which influences our daily lives. Thanks to the development of high performance materials, large area production and integrated technologies, significant efforts have been made to develop high performance photodetector arrays (PDAs) in order to satisfy growing demands on new innovate optoelectronic device applications including motion and position detection [1], imaging [2], and spectrophotometry [3]. In this regard, a diverse range of materials and different structures have been investigated and tailored for different photo-detection applications with specific requirements such as spectral range, speed and sensitivity.

Contrary to conventional metal/semiconductor (MS) type Schottky junction photodetectors (PDs), where the Fermi level of metal electrode remains unchanged due to high density of states, the Fermi level of graphene can be shifted towards either lower or higher energy states relative to its Dirac point simply by electrostatic gating and/or charge transfer doping from an external source [4]. Accordingly, PD architecture based on a graphene/silicon (GSi) heterojunction have attracted a great deal of attention in the last decade. It has been shown that a rectifying Schottky contact with an energy barrier level of around 0.5–0.8 eV is formed when graphene is laid on the surface of bulk Si substrate [5]. The strong rectification between GSi heterojunction enables the highly sensitive, self-powered and relatively fast PDs with respect to the p-n or p-i-n counterparts in the visible and short wavelength infrared spectral ranges [6]. The GSi heterojunction operates as a Schottky barrier diode, which is sensitive to light in the spectral range between 400 and 1100 nm due to the bandgap of Si. When graphene is employed as an electrode on Si, it does not only act as an optically transparent conductive layer, but it functions also as a photon absorbing active material similar to metal silicide electrodes used in conventional metal/Si Schottky barrier PDs [7, 8]. Under light illumination, although a large amount of photons is converted into photogenerated charge carriers in Si, the optical absorbance in graphene (2.3%) contributes to light detection as well through internal photoemission over the Schottky barrier. The photogenerated electrons with high enough energies to

overcome the Schottky barrier are accelerated toward the bulk of Si due to the built-in electric field at the interface of GSi. As the electrons pass through the depletion region of Si, they undergo energy loss processes that prevent them from passing back into the graphene over layer. This results in an effective charge separation and, hence, in a measurable photocurrent and/or photo-voltage even under zero-bias (self-powered) conditions. A variety of different design strategies have been employed to fabricate single element GSi based Schottky barrier PDs. These include the transfer of monolayer graphene either on oxide-free or on the nanotip patterned surface of bulk Si substrates [9, 10]. There are several other approaches relying on the fabrication of these types of PDs using silicon-on-insulator (SOI) technology. A SOI structure, which is composed of buried SiO_2 (BOX) sandwiched between a thin Si layer and a thick Si substrate, provides great opportunities for producing GSi based PDs with improved device performance. For example, a bottom-gated SOI transistor with isolated patterned graphene layers on top of a single channel Si has been utilized as a single pixel PD to detect light in the visible to the near infrared range [11]. In a subsequent work, it has been shown that SOI based single pixel GSi Schottky PDs exhibit a maximum spectral responsivity (R) of around 0.26 AW^{-1} at 635 nm peak wavelength and a response time substantially smaller than a microsecond compared to their counterparts fabricated on bulk Si substrates [12].

Recent advances in Si PD technology allows several opportunities for the design of multi-element PDAs with small element size and narrow pitches between adjacent elements [13-15]. Besides, linearly aligned one-dimensional (1D) PDAs, Si based two-dimensional (2D) PDAs, which comprises an x-y axis aligned mosaic-like device structure, have been studied so far [16]. Much interest in 2D PDAs derive from their potential to deliver the next generation of flat and passive matrix image sensors [17]. These devices operating as active or passive mode consists of a photosensitive layer sandwiched between a transparent anode and a cathode. A passive matrix image sensor results by patterning the anode into columns and the cathode into rows to form an array of pixels from the intersections between the cathode and anode electrodes. In general, Si based 2D passive matrix PDA need external bias for light detection on the pixel shared by the two electrodes [18].

Self-powered 2D passive matrix PDA based on the integration of conventional semiconductors and 2D materials is thought to attract great of interest in the area of image sensing due to energy-efficiency and its ease of fabrication. Graphene as a conductive 2D material provides new opportunities for photonic devices with exceptional electronic and

optical properties. Researchers showed that graphene can be used as stretchable transparent conductive electrode (TCE) in active [19, 20] or passive [21] matrix display technology. For instance, in one study, Park et al. demonstrated that graphene can be integrated into organic light emitting diodes (OLEDs) by connecting the source electrode of the thin film transistor (TFT) to the anode of the OLED, thus demonstrating pixel-by-pixel driving through a 2D TFT array in an active-matrix configuration [20]. In another study, Salihoglu et al. stated that graphene-based passive matrix fluorescent display can be fabricated by gate tunable quenching of quantum dots (QDs) for new type of hybrid displays and color-variable devices working in the visible spectrum [21]. In another study, Goossens et al. investigated that monolithic integration of graphene with a Complementary Metal Oxide Semiconductor (CMOS) integrated circuit phototransistor operating as a high-resolution, broadband image sensor and operate it as a digital camera that is sensitive to ultraviolet (UV), visible and infrared (IR) light (300 – 2.000 nm) [22].

Si based PDs can arrange into Si units by stacking them one by one in a row but one of the substantial problem faced in such PDA is the optical crosstalk. Optical crosstalk includes the effect of photon refraction, reflection at boundaries, and external and internal scattering in detector arrays. As the PD size and the pitch (distance between PDs) of the detector array get smaller, there is a greater probability of crosstalk influencing system performance since the probability of a photogenerated carrier being collected by a neighboring junction increases. This situation causes the increment in the device noise, therefore, detection sensitivity of detector decreases accordingly. When the incident light on one element in PDA is coupled to neighbor one by reflection or by lateral diffusion of photogenerated charge carriers [23], optical crosstalk occurs due to the illumination technique and array geometry [24]. Apart from these, optical crosstalk can also appear with different doping concentration of the active junction layer [25] and can be controlled with the arranging the distance between the elements and the thickness of the device layer (i.e., absorption layer) [24] in different types of PDAs. In literature, there are lots of researches in the field of decrement in optical crosstalk effect of devices. Menon et al. has been theoretically investigated that optical crosstalk can be decreased as distance between electrodes and the absorption layer thickness are increased for Si based interdigitated lateral p-i-n photodetector (ILPP) array devices [24].

In order to further minimize the possible optical crosstalk between neighboring elements and hence decrease the dark current in junction, it has become important to separate and disconnect individual graphene electrodes on every single Si element in the

array and examine the device performances. In literature, disconnected and separated graphene arrays can be patterned laterally on desired substrate using soft-patterning technique developed in Ref. [26] or inject printing method which represents performance and cost effectiveness in fabrication route. Recently, Grillo et al.[27] showed that the four parallel graphene ink and Si heterojunction based diode arrays with Si *common* electrode can be manufactured on commercial heavily doped Si substrates using 'scratch and print' approach. In that study, Si is used as *common* electrode and the optical crosstalk between the diodes is inevitable due to the fact that photo-generation occurs mainly at the Si surface [28]. To the best of our experience, optical crosstalk problem can be eliminated in graphene and Si based PDA fabrication in the following manner; (i) using graphene as *common* electrode, or (ii) individually patterning graphene electrodes on a single substrate using SOI technology. Besides the conventional fabrication routes for Si array packaging, it has been shown that SOI structure enables well isolated Si units in a single substrate using standard microfabrication techniques, hence optical crosstalk between elements can be minimized using this technology [29]. SOI technology plays an important role to configure multiple PDs on single Si substrate. SOI structure consists of a thin single crystal Si film on amorphous SiO_2 layer and handle Si, respectively. The BOX layer reduces leakage currents and provides full dielectric isolation between device and handle Si layers. This opportunity also improves the detection limits, and thus decreases the probability of the optical crosstalk between Si channels. Moreover, the use of SOI in the fabrication of PDA ensures remarkable advantages in regards to electrical leakage in sandwiched structure because the BOX also behaves as etch stop layer [29].

The motivation and scope of this thesis lies in the investigation of the novel graphene and SOI integrated 1D and 2D PDAs working with hybrid absorption mechanism, broadband operation, high *R* and fast recovery time together with ease of fabrication. Different from previous studies in the literature, we systematically fabricated a multi-channel GSi Schottky barrier PDAs with *common* graphene electrode and compared them with a typical G/n-Si based reference PD fabricated on a bulk n-Si (500 μm thick) having the same doping concentration as the n-Si layer on the SOI substrate under zero bias conditions. Subsequently, we separated graphene electrodes on PDA structure and compared the optical crosstalk effect occurred in PDAs with *common* and *separate* graphene electrode. In addition, we also fabricated a 2D pixel PDA with significant reduction of optical crosstalk using individual graphene electrodes.

The experimental findings presented in this thesis are expected to offer exciting opportunities in terms of high value-added GSi based PDA device applications such as multi-wavelength light measurement, level metering, high-speed photometry, position/motion detection and image sensing.

The structure of the thesis can be summarized as follows. Chapter 1 explains our motivation behind this work by relating the properties of GSi Schottky junction with our aim. Chapter 2 gives a brief account of the basics of SOI technology and graphene and also presents more specifically GSi heterojunction PDs and their fundamental operating principles. Chapter 3 focusses on the fabrication routes and methods used for the characterization of the devices that have been developed in the context of this thesis. Chapter 4 presents the experimental results and the discussions. Chapter 5 provides a conclusion of main findings from the experiments.

CHAPTER 2

BACKGROUND

This chapter explores the basics of SOI technology and the fundamental properties of graphene by introducing its physical and electronic structure and how they give rise to novel electronic and optical properties and also describes various methods utilized for graphene synthesis. In addition to this, the physics behind the mechanism of the MS junction, and more specifically GSi heterojunction PDs and their fundamental operating principles will be reviewed while introducing the relevant terminology and essential figures of merit for PDs.

2.1. Fundamentals of SOI technology

A typical SOI substrate is designed with high precision for the purpose of creating multilayer semiconductor and dielectric structures. This enables the manufacturing of advanced Si devices with novel functionalities. SOI substrates are comprised of a thin layer of Si that is electrically isolated from the bulk Si by a layer of BOX. The material used for the buried oxide layer is usually sapphire, although more recently silicon dioxide (SiO_2) has been used as well. The isolation of the device layer from the substrate leads to a significant reduction in junction capacitance and leakage current in SOI substrates. This, in turn, enhances the switching speed of Si-based devices and reduces their power consumption [30]. High energy consumption of bulk Si devices is a critical limitation, which has brought SOI into the focus of interest. Consequently, this technology has become a mainstream feature of the semiconductor electronics roadmap, thanks to its extended scalability and superior performance, including higher speeds and lower power dissipation.

One of the most significant benefits of SOI technology is its capability to serve as a photonics platform. It provides significant benefits in terms of the design, fabrication, and performance of microelectromechanical systems (MEMS) and CMOS integrated semiconductor devices [31]. This technology enables the monolithic integration of optics and electronics onto a single substrate [32]. Lowering the operating voltage of SOI-based

devices is an alternative method of reducing their power consumption while maintaining their performance. Additionally, SOI substrates offer several benefits in micro-optical systems, mainly due to the substantial index difference between Si (n= 3.45) and SiO_2 (n= 1.46). The slanted surfaces of SOI substrates allow incident light to propagate, and the light rays can be confined at the top Si-BOX interface through total internal reflection. These unique structural properties may have a significant impact on the future of Si-based technology, as they could pave the way for the development of new SOI-based devices with widespread implications.

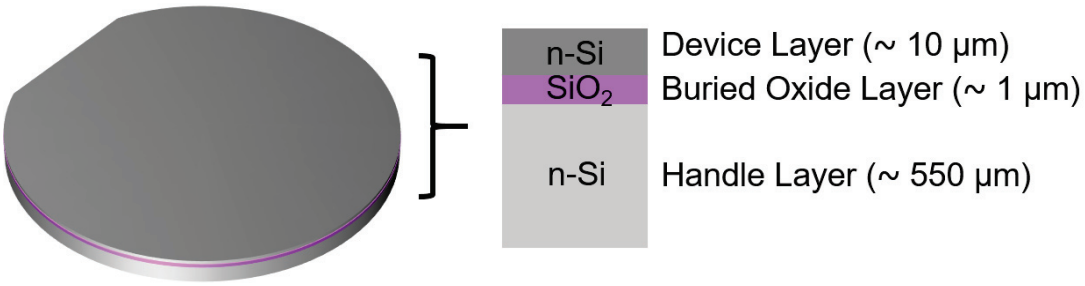


Figure 2.1. The structure of a typical SOI wafer used in the design and fabrication of PDAs devices for our studies.

SOI wafers are composed of three layers as shown in Figure 2.1. Si as device layer, SiO_2 as insulating layer and Si as handle layer combine to form SOI structure. SOI wafers can be manufactured by using several techniques such as Separation by Implantation of Oxygen (SIMOX) [33], SmartCut [34] and Etchback SOI (BESOI) [35]. Production techniques depend on the topmost Si layer thickness. For thick (>1 µm) Si device layer, the BESOI method is generally used and top-Si layer is obtained by back-grinding and polishing processes as seen Figure 2.2. Fusion bonding technique is generally used in the production of BESOI. This technique involves pressing two highly polished wafers together at room temperature (R.T.), causing them to adhere to each other. This processing method is particularly useful in optoelectronics and MEMS applications because it allows for the creation of relatively thick device and oxide layers. A thermally oxidized wafer or a handle wafer is fused to pure Si, or donor wafer in this method. The donor wafer is then carefully cleaved or thinned to achieve the required device layer thickness.

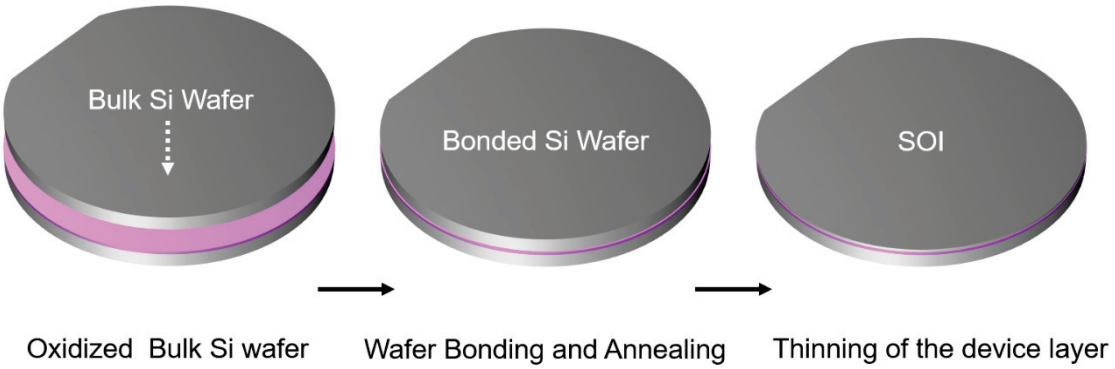


Figure 2.2. A schematic representation of the BESOI process [36].

As noted earlier, devices fabricated using SOI structures are distinct from conventional devices fabricated out of bulk Si. This is because SOI structures are constructed on top of electrical insulators, which are typically made of SiO_2 or sapphire. Devices made in this way are often referred to as silicon-on-sapphire (SOS). The selection of insulating material is largely determined by the intended application. For high-performance radio frequency (RF) and radiation-sensitive applications, sapphire is often used. On the other hand, for microelectronic devices that require reduced short-channel effects, SiO_2 is typically preferred [37].

2.2. Graphene

In the recent years, graphene, a two-dimensional (2D) allotrope of carbon arranged in a honeycomb structure [38], has garnered significant interest due to its exceptional electronic and optical characteristics. Some of its notable properties include high electron mobility, an atomic-thin structure, and broad-spectrum absorption spanning from UV to terahertz (THz) frequencies [39]. These features are attributed to graphene's linear dispersion relation and its unique zero bandgap characteristic. Moreover, graphene has high charge carrier mobility [40] and tunable optical and electrical properties via electrostatic gating and chemical doping [41]. In addition, graphene exhibits high sensitivity through adsorbates due to the large surface-to-volume ratio [42]. Given these exceptional properties, graphene has emerged as a prime candidate for multifunctional technology applications in various fields, including imaging and sensing, communication and spectroscopy, chemical and biological sensing, as well as PDs and solar cells.

2.2.1. Atomic structure of graphene

Graphene refers to a single layer of graphite are composed of carbon atoms that are sp^2-hybridized, arranged in a hexagonal honeycomb structure and the weak van der Waals bonds as illustrated in Figure 2.3 (a). These bonds are responsible for holding together each monolayer of graphene in graphite [38]. In a flawless graphene sheet, each carbon atom forms covalent bonds with three adjacent carbon atoms. Carbon has four valence electrons in its outermost shell, which can participate in covalent bonding with other atoms. In a graphene lattice, each carbon atom has three outer electrons in its atomic orbitals of 2s and 2p. These three electrons participate in covalent bonding with the neighboring carbon atoms, forming three σ-bonds and one π-bond. In a graphene lattice, each carbon atoms occupy the atomic orbitals of $1s^2$, $2s^2$, and $2p^2$. Two electrons are located in the inner shell and do not contribute to the conductivity of graphene. Figure 2.3 (b) shows the sp^2 hybridized orbitals of carbon atoms symmetrically distributed in the x and y plane at angle of 120^o forming three σ-bonds. The remaining four electrons are in the outer shell and occupy the orbitals of 2s and 2p ($2p_x$, $2p_y$, and $2p_z$). The sp^2 hybridization occurs when three orbitals, s, p_x, and p_y combine together. As seen in Figure 2.3 (b), the p_z orbital is perpendicular to the plane and forms a weak π-bond, while the bonding between p_x and p_y electrons is known as the σ-bond in graphene [43]. The σ-bonds are formed by overlapping of the hybridized sp^2 orbitals of the carbon atoms and they are the reason behind the extraordinary mechanical robustness and elasticity of graphene, while the π-bond is formed by the unhybridized p orbital that is perpendicular to the plane of the graphene sheet. The remaining p orbitals of each carbon atom contribute to the delocalized π-electron system, which is responsible for the high electrical conductivity of graphene. Monolayer graphene has a thickness of 0.335 nm and the distance between the nearest carbon atoms in graphene is 0.142 nm (see Figure 2.3 (a)).

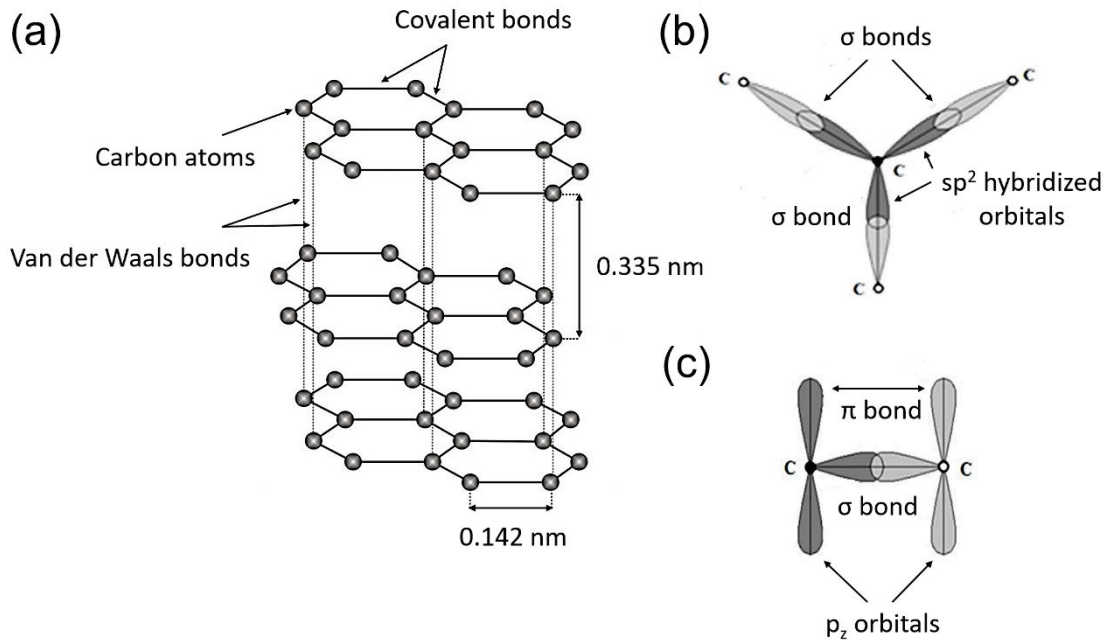


Figure 2.3. Structure of graphene. (a) Graphene layers held together by van der Waals bonds in graphite. (b) In-plane bonds and (c) out of plane bonds. (Adapted from: [44]).

Figure 2.4 (a) illustrates the hexagonal lattice structure of graphene, which contains two carbon atoms per unit cell, namely A and B. The real space lattice vectors of a_1 and a_2 can be written as following,

$$a_1 = \frac{a}{2}\left(3, \sqrt{3}\right), \qquad a_2 = \frac{a}{2}\left(3, -\sqrt{3}\right) \tag{2.1}$$

where a is the lattice constant with a value of 0.246 nm. The first Brillouin zone of the reciprocal lattice is depicted Figure 2.4 (b), with the center point denoted as Γ, and the two non-equivalent corner points indicated as K and K'. The M point denotes the center of the edge of the hexagonal Brillouin zone (BZ).

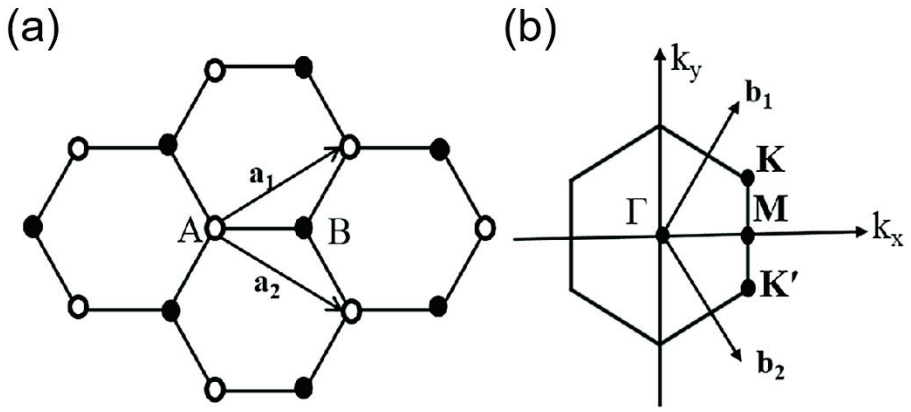


Figure 2.4. Lattice structures of graphene. (a) Honeycomb lattice structure of graphene in real space with a basis of two atoms A and B. (b) First Brillouin zone of graphene showing the high-symmetry points (Source: [45]).

The first Brillouin zone of graphene in reciprocal space is defined by the lattice vectors b_1 and b_2;

$$b_1 = \frac{2\pi}{3a}\left(1, \sqrt{3}\right), \qquad b_2 = \frac{2\pi}{3a}\left(1, -\sqrt{3}\right) \tag{2.2}$$

These corners K and K', also known as Dirac points, are of particular significance in the physics of graphene. Their positions in momentum space are given by,

$$K = \frac{2\pi}{3a}\left(1, \frac{1}{\sqrt{3}}\right), \qquad K' = \frac{2\pi}{3a}\left(1, -\frac{1}{\sqrt{3}}\right) \tag{2.3}$$

At these Dirac points, that have two different sets. Each of them is non-equivalent and included three Dirac points. Fermi level of pristine graphene lies completely at the Dirac points, and hence graphene can be regarded as a gapless semiconductor or a zero-overlap semimetal. The electron dispersion around the Dirac points is linear instead of parabolic as most of semiconductors.

2.2.2. Electrical properties of graphene

The electrical properties of graphene arise from the behavior of the π-electrons in the carbon atom. In the honeycomb lattice structure of graphene, the bonding between the carbon atoms is governed by the energy levels of the π-bond orbitals. The lower energy π-bonds form the valence band, while the higher energy anti-bonding π* electrons form

the conduction band. The corners of the BZ, *K* and *K′*, are of particular importance as the unique physics of graphene arises from these points, which are known as Dirac points. The conduction and valence bands in graphene have a cone-shaped dispersion and meet at six symmetric points in the first Brillouin zone, which are known as Dirac points. These points are labeled as *K* and *K′* and are shown in Figure 2.5 (a). Here, the z-axis represents the energy $E(k)$, with the xy-plane corresponding to the momentum $k = (k_x , k_y)$.

The valence (π) and conduction ($\pi*$) bands of monolayer graphene intersect at the Dirac points, which define the Fermi energy (E_F). This unique band structure results in graphene being classified as a semi-metal or zero-bandgap semiconductor. The energy dispersion around the Dirac points can be expressed as a linear equation [46].

$$E(k)^{\pm} = \pm\hbar\, v_f\, |\mathbf{k}| = \pm\hbar\, v_f \sqrt{k_x^2 + k_y^2} \qquad 2.4$$

where $\hbar$ is the reduced Planck constant, k is the wave vector in spherical coordinates and v_f is the Fermi velocity. The linear energy dispersion relation around the Dirac points in graphene makes the Fermi level highly sensitive to external influences such as electric fields, mechanical strains, and chemical doping. The Fermi level can be shifted by applying a gate voltage or by chemical doping, which can be used to tune the electrical properties of graphene for various applications. The sensitivity of the Fermi level also makes graphene an excellent platform for studying various physical phenomena, such as quantum Hall effect and topological insulators [47].

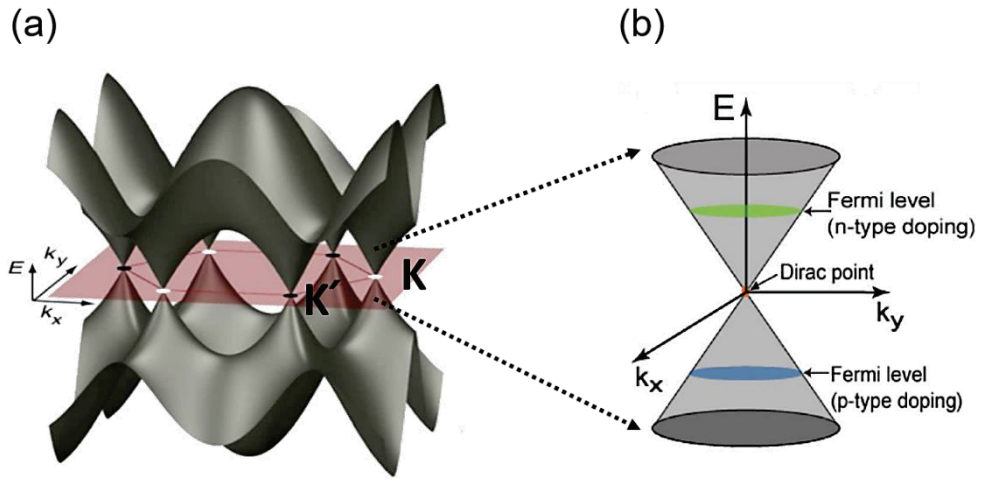


Figure 2.5 (a) Graphene 3D band structure obtaining from tight binding method and (b) zoom in to low-energy linear dispersion as two cones touching at the Dirac point [48].

Due to the linear dispersion relation of energy bands around the Dirac point, graphene exhibits a zero-energy bandgap, and the Fermi level for undoped graphene is located at the Dirac points where the up and down side of one Dirac point corresponds to conduction and valance band, respectively. As a result, graphene is classified as a semi-metal or a zero-gap semiconductor. Graphene's suitability for various electronic and optoelectronic applications can be enhanced by its ability to adjust the position of the Fermi level using external factors, such as doping or an electric field. Unlike most semiconductors, which display parabolic dispersion, the energy dispersion relation of graphene near the Dirac points exhibits linear behavior.

Under non-equilibrium conditions, such as an applied electric field, or in the presence of impurity atoms, the E_F level can shift away from its equilibrium value of 0 eV [49]. The E_F in graphene can be related to the carrier density (n) by $E_F = \hbar v_f \sqrt{\pi n}$. This means that it is possible to control the E_F by adjusting the carrier density (which includes both electrons and holes) through a bias gate in a graphene-based field-effect transistor. Depending on the position of the E_F with respect to the Dirac point, either electrons or holes can be the majority carriers in graphene. In graphene, whether electrons or holes are the majority carriers depends on the position of the E_F relative to the Dirac point (as shown in Figure 2.5 (b)). Manipulating the majority of either n-type or p-type carriers can result in an ambipolar effect, whereby the Fermi level can be altered [50].

Table 2.1. Comparison of electrical properties of graphene with other conductive materials [51].

Material	ρ (Ω.m) at 20°C	σ (Sm^{-1}) at 20°C
Graphene	1.00×10^{-8}	1.00×10^{8}
Silver	1.59×10^{-8}	6.30×10^{7}
Copper	1.68×10^{-8}	5.96×10^{7}
Gold	2.44×10^{-8}	4.10×10^{7}
Aluminum	2.65×10^{-8}	3.77×10^{7}

The resistivity and conductivity of highly conductive materials are listed in Table 2.1. Graphene's electric conductivity exceeds that of silver (Ag), copper (Cu), and aluminum (Al) by 37%, over 40%, and 62%, respectively. These findings indicate that graphene holds great potential as a conducting material. Besides, the bandgap exists in the monolayer form and remains essentially the same in bulk form in traditional

semiconductors, whereas in graphene, the bandgap increases as the number of layer increases. This is because the interlayer coupling between adjacent layers lifts the degeneracy of the energy bands, leading to a deviation from the linear dispersion of monolayer graphene and the opening of a bandgap. The magnitude of the bandgap depends on the number of layers and the stacking arrangement, making it possible to tune the electronic properties of graphene by controlling its layer thickness and stacking order. For monolayer graphene, the valence and conduction bands touch at the six Dirac points, resulting in a zero bandgap and a linear dispersion relationship between energy and momentum and also these bands do not overlap due to a zero density of states. This linear dispersion relationship is a unique feature of graphene and this feature is responsible for its exceptional electronic properties, such as high carrier mobility. However, as the number of graphene layer increases, the band structure deviates from linear dispersion.

2.2.3. Optical properties of graphene

Graphene has zero bandgap and symmetrical energy bands. Its unique band structure contributes to remarkable optical properties. The simplicity of the band structure also makes it easy to measure the material's absorption spectrum. A monolayer of graphene has a broad absorption spectrum, ranging from UV to THz wavelengths. Although the absorption spectrum of graphene is almost constant with an absorption coefficient of $\pi\alpha \cong 2.3 \pm 0.10\%$, where α is the fine structure constant [52] between wavelengths of 300 nm to 2500 nm due to the linear band structure of graphene at low energies, there is a slight deviation from the expected $\pi\alpha$ absorption at higher frequencies. This deviation is caused by nonlinearities in the band structure [53].

The optical absorption in graphene arises from two processes: interband and intraband transitions. Intraband transitions occur at low photon energies, ranging from far-infrared (FIR) to THz, while interband transitions dominate at higher photon energies, such as in the mid-infrared (MIR) and UV spectral regions. In intraband transitions, the optical absorbance is primarily supplied by free carriers in graphene. On the other hand, interband transition in graphene refers to the process where photoexcited electrons undergo direct transitions from the valence band to the conduction band, which dominates the optical response at higher frequencies. For instance, the optical conductivity of pristine graphene at zero temperature is frequency-independent due to the linear band

structure, and it is proportional to the α and v_f. Nair et al. showed that monolayer graphene can absorb approximately 2.3% of incident light over the visible spectrum (400-750 nm), which is attributed to $\pi\alpha$ based on the Dirac cone approximation [54]. The approximation, however, is only valid for the coupling between light and relativistic electrons that are in close proximity to the Dirac point [55].

To clarify, the universal absorption of graphene has been experimentally confirmed on a suspended graphene sample, as shown in Figure 2.6 (a). This high absorption value is remarkable, especially considering the fact that graphene is only a single atom thick [53]. Figure 2.6 (b) shows the dependence of optical absorbance on the number of graphene layers. The absorbance per layer is not constant but rather decreases as the number of layer increases. For instance, graphene's optical absorption is directly proportional to the number of layers present, where each layer absorbs 2.3% of incident light across the visible spectrum.

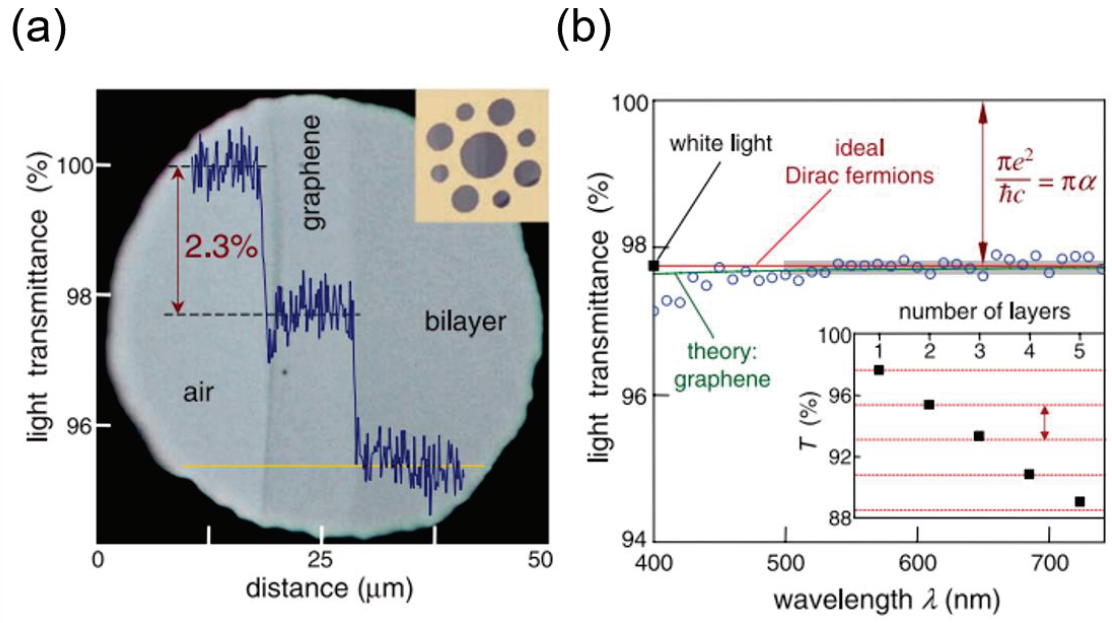


Figure 2.6 (a) A photograph of a single layer and bilayer graphene suspended over a 50 μm aperture taken under white light and the scan profile shows the intensity of transmitted white light along the yellow line. The inset shows the sample design with a set of apertures. (b) Transmittance spectrum of single layer graphene in the visible range. The inset shows the linear decrease in the transmittance as the number of layer increases. (Taken from Ref. [54])

Graphene's excellent optical transparency in the UV, visible, and near infrared (NIR) regions makes it an ideal candidate for use as a TCE in optoelectronic devices. TCEs are used as a replacement for traditional indium tin oxide (ITO) electrodes.

Graphene's high electrical conductivity, combined with its optical transparency, makes it an attractive alternative for use in applications such as solar cells, touchscreens, and flexible displays [56]. For example, ITO is a commonly used material in such devices, but this material is expensive, brittle and exhibits a transmittance of less than 80% at wavelengths around 600 nm as depicted in Figure 2.7. Due to its high transparency level of 97.7%, a monolayer graphene layer has a significant advantage over ITO in the detection of visible light. Therefore, graphene, with a transparency of over 90% in the range of 0.4 – 1.3 μm, is a strong contender to be used as a TCE in both photovoltaic devices and PDs that function in the visible and NIR regions.

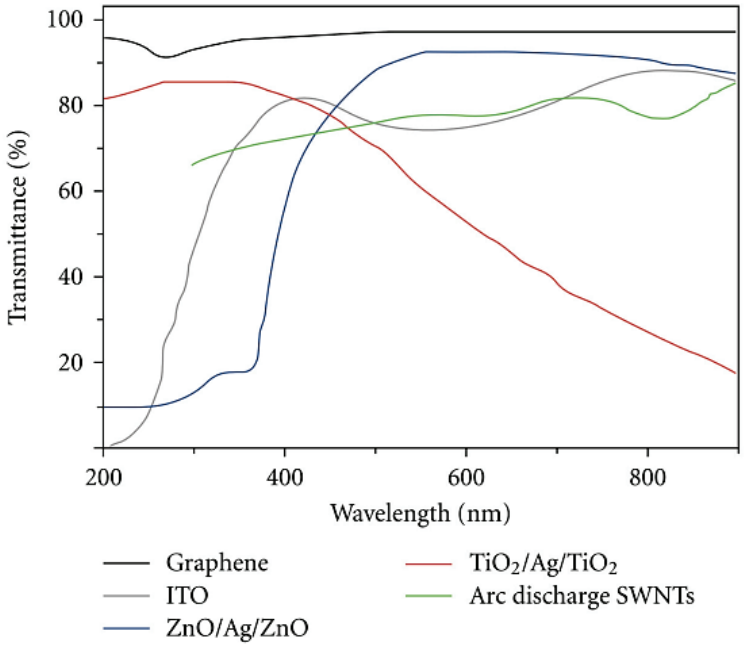


Figure 2.7. The transmittance of various TCEs that are used commercially for UV, visible and NIR regimes [57].

2.2.4. Production of graphene by chemical vapor deposition method

High-quality graphene plays a crucial role in electronic and optoelectronic devices. Several methods have been utilized to achieve this objective, and the most commonly used techniques are classified into three categories; i) mechanical exfoliation, ii) thermal decomposition of silicon carbide (SiC), and iii) chemical vapor deposition (CVD). The selection of a specific method depends on the intended application and the

devices where graphene will be used. Additionally, each technique has its own set of advantages and drawbacks, such as production cost, yield, and other factors.

While graphene can be prepared by several techniques like mechanical exfoliation method [43], chemical exfoliation of graphite oxide [58] or epitaxial growth on SiC [59], CVD has appeared as an essential way for the preparation and production of graphene since it was first reported in literature [60]. High quality graphene based on crystallite size and mobility can be achieved by mechanical exfoliation method, however, sample size is limited. Although epitaxially grown graphene on SiC has a high quality than exfoliation method does, high temperature, high cost of production and lacking of transferring graphene on another substrate are limited this method for applications. In terms of transferring process of graphene on another substrate makes CVD method more practical and also CVD synthesized graphene has high quality, large area produced and defect free graphene is possible with this method. Therefore, graphene produced by CVD has greater interest.

CVD is the most commonly used method for growing graphene, which involves a chemical reaction of a vapor near or on a heated surface. This technique can produce high-quality and single-layer graphene on a large scale. A typical CVD system consists of a transition metal foil (such as copper (Cu)), a supply of carbon-containing gas (such as methane (CH_4)), and a reaction chamber that can operate at temperatures up to 1200 °C. In the CVD process, CH_4 reacts with metal catalysts at high temperatures (~ 1000 ^oC) to produce graphene.

Figure 2.8 provides a schematic diagram of the CVD process for producing graphene from CH_4 and hydrogen (H_2). Graphene domain size and shape can be controlled by additional H_2 flow as an etching reagent and the catalytic activity of the Cu surface. The diagram highlights each step in the process for clarity. Transport of reactants by convection in the gas flow initiates this process (step 1), pursued by their thermal activation (step 2). The reactants are subsequently moved across the stationary boundary layer by gas diffusion from the main gas stream (step 3). Subsequently, the reactants are either adsorbed onto the surface of the substrate (step 4) or diffused into the bulk of the substrate (step 5), depending on the solubility of carbon. During the surface processes (step 6), catalytic decomposition of reactive species occurs in addition to surface migration to attachment sites and other heterogeneous reactions. After film growth, the by-products are desorbed from the substrate (step 7) and diffused through the boundary

layer to the main gas stream (step 8). They are then carried away by the force of convection to the exhaust system (step 9) [61].

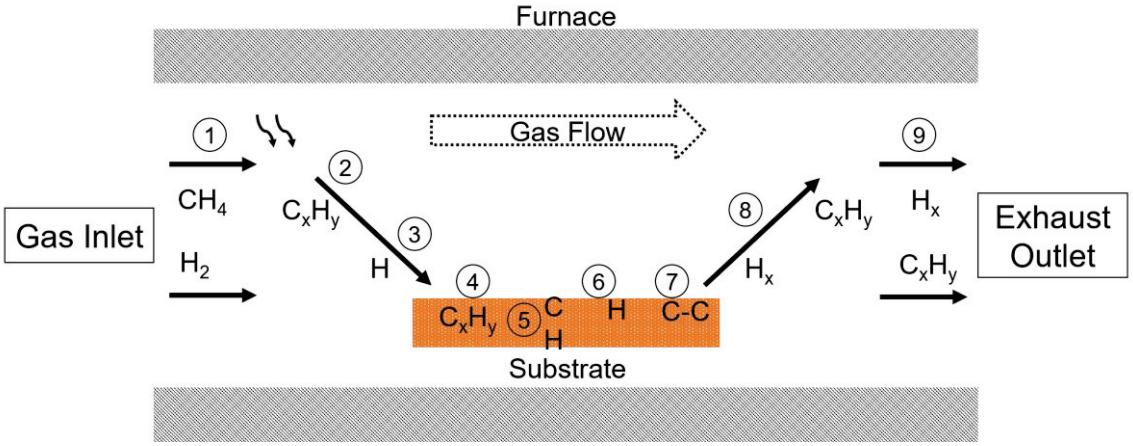


Figure 2.8. A demonstration of CVD grown graphene process under gas mixture of CH_4/H_2 on a substrate consists of nine main steps.

As a substrate, generally transition metals, such as Cu and Ni have been utilized as catalysts in the growth of graphene due to their cost and easy process ability. However, Cu is more eligible compared to Ni due to its low carbon solubility (~0.03 at % [62]) which plays an important role to control the number of graphene layers. Due to this low solubility, Cu and carbon generate a weak bond through charge transfer from the π electrons in the sp^2–hybridized carbon to empty 4s states of Cu [63]. Therefore, graphitic carbon forms easily with this combination of very low affinity between carbon and Cu. As seen in step 5 of Figure 2.8, graphene growth occurs on the Cu surface where CH_4 is catalytically decomposed, and carbon atoms are adsorbed to form a graphene film. On the other hand, if Ni is used as the catalytic substrate, carbon atoms are diffused into the deep of Ni, and graphene growth happens during the cooling step when carbon precipitates to the surface. To avoid the formation of multi-layer graphene on high carbon soluble substrates, fast cooling is recommended.

It is also known from the literature that large size graphene up to 30 inches can be synthesized with controllable parameters by using CVD method [64]. Moreover, graphene layers grown by CVD has strong p-type carrier density since therefore its fermi level is below Dirac point [65]. The theoretical limit of graphene's carrier mobility (μ) is about 2×10^5 $cm^2/V.s$ at carrier densities on the order of a few 10^{12} cm^2 at R.T.[66]. This predicted

high mobility is experimentally obtained at R.T. was determined by Hall effect measurement on exfoliated graphene sandwiched in hexagonal boron nitride (h-BN) sheets under a low carrier density of about 10^{11} cm^2 [67].

2.3. Physics of Schottky junction

The MS junction has been a key factor in advancing semiconductor device technology, owing to its straightforward fabrication process that has been used for decades. When a metal and a semiconductor are brought into close contact, a potential barrier is created at their interface, which is primarily based on the Fermi level of the semiconductor and the work function of the metal (Φ_m) [68]. At the interface between a metal and a semiconductor, there is a potential barrier that can have varying height and shape, which governs the flow of current between the two materials [69]. This potential barrier can result in two types of devices: Ohmic, where the barrier is negligible and current flows easily, or rectifying (also known as Schottky), where the barrier is significant and current flows only in one direction [70] (see Figure 2.9). In Ohmic contacts, the potential barrier at the MS interface is very thin, and charge carriers can effectively flow through the interface via a quantum tunneling process [68]. This results in linear current-voltage behavior and lower resistance, which follows Ohm's law. Ohmic contacts are typically achieved through metal contacts built on a highly doped semiconductor [70], where the doping level is high enough to ensure that the contact resistance is low and the current flows freely [68].

Schottky junctions are also called rectifying junctions because they exhibit rectification behavior, where current flows easily in one direction (forward bias-ON state) but not in the opposite direction (reverse bias-OFF state). In forward bias, the applied voltage reduces the potential barrier at the MS interface, allowing the charge carriers to easily flow through the junction. In reverse bias, the potential barrier increases, leading to a decrease in the current flow through the junction. The rectifying behavior of Schottky junctions makes them suitable for rectifiers and detectors.

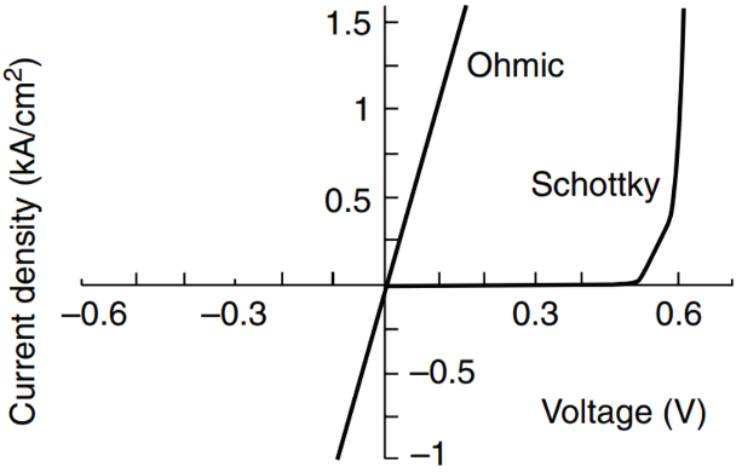


Figure 2.9. A comparison for I-V graphs of a resistor and a diode. The linear (resistor) and non-linear (diode) I-V characteristics represent the ohmic and Schottky contacts, respectively. (Source: Ref.[71])

Schottky junction diodes in their early forms were primarily developed through empirical research, as their performance was closely related to the fabrication process. However, over the course of several decades, advancements in metal contact deposition technologies led to the production of more dependable and consistent Schottky junction diodes. Although significant experimental progress was made in the field, the comprehension of the charge transport nature at MS contacts progressed at a slow pace. The rectifying properties of the MS junction were initially demonstrated by Braun in 1875 [72], and later, Schottky [73], and Mott [74] elucidated the physical mechanism behind the formation of the barrier, and constructed models to explain the shape of the barrier and current transport. These models, currently known as the diffusion theory, are widely recognized in the field. While the diffusion theory provides insight into the direction of rectification, it falls short in explaining the current limiting mechanism at the junction and provides inaccurate predictions for the barrier height. Bethe in 1942 [75] presumed that the majority carriers (electrons for n-type semiconductors) dominate the current and possess sufficient kinetic energy to overcome the potential barrier at the MS interface. This model is known as the thermionic emission (TE) model, and the current resulting from electron transport over the potential barrier is referred to as the thermionic current. Due to this physical phenomenon, MS diodes find wide applicability in various technological fields, including but not limited to sensors, solar cells, and PDs [76].

The characteristics of MS diodes, such as Schottky barrier height (SBH), ideality factor (η), series resistance (R_S), and speed, are largely determined by the interface properties and the selection of the metal and semiconductor combination. While the state-of-the-art high vacuum systems enable the production of more reliable and reproducible MS diodes, achieving a perfectly intimate MS junction remains a challenge due to surface and interface states. Thus, the characteristics of MS diodes remain strongly dependent on the fabrication procedure [10].

In the following sections of 2.3.1, 2.3.2, 2.3.3 and 2.3.4, we will introduce the energy band diagram and charge transport mechanism of MS Schottky junctions. Additionally, we will extract key diode parameters, such as the η and SBH (Φ_B), from the current-voltage (I-V) characteristics of the MS junction.

2.3.1. Ideal conditions at the MS interface

The electronic properties of the chosen thin films and substrates are closely linked to the characteristics of the MS junction. When appropriate materials are selected, an ideal case can be achieved, resulting in either ohmic or rectifying characteristics for the MS junction [70]. Matching the Φ_m with the electron affinity (χ) of the semiconductor, along with ensuring similar doping concentrations between the two, can result in a good approximation for the ideal case. The work function of a material is the amount of energy required to move an electron from the E_F to the vacuum level (E_{VAC}), which represents the energy level of an electron that has completely escaped the material's surface. In a metal, E_F represents the highest energy level that electrons can occupy at absolute zero temperature. The Φ_m can be affected by the presence of a dipole layer or surface contaminations on the metal thin film surface, which can cause changes in the work function [69]. The Fermi level in semiconductors ($E_{F,S}$) changes with the doping concentration. In n-doped Si, for example, E_F is closer to the minimum of the conduction band (E_C) (which is called as χ and it is about 4.05 eV away from E_{VAC} for Si). This means that the work function of a semiconductor (Φ_{SC}) is not a fixed value. In contrast, the χ of a semiconductor is defined as the energy difference between the E_{VAC} and the E_C, and remains constant for a given semiconductor, regardless of doping concentration. Similar to the Φ_m, χ is an intrinsic property of a semiconductor and does not change with doping level. However, the electronic properties of semiconductors can still be affected

by factors such as the thin film deposition method, surface morphology, and other deposition conditions, which can result in slight differences in their electronic properties.

Table 2.2 provides a comparison between ohmic and Schottky junctions based on Φ_m and Φ_{SC}. If the Φ_m is higher than that of the n-type semiconductor, a Schottky junction is formed. On the other hand, if the Φ_m is lower than that of the p-type semiconductor, a Schottky junction is also formed. In all other cases, an ohmic junction is formed between the metal and semiconductor.

Table 2.2. The comparison of work functions in MS junctions.

	n-type semiconductor	p-type semiconductor
$\Phi_m > \Phi_s$	Schottky	Ohmic
$\Phi_m < \Phi_s$	Ohmic	Schottky

Figure 2.10 illustrates an example of rectifying behavior between a metal and an n-type semiconductor assuming an ideal case without interface states or other anomalies. Figure 2.10 (a) shows energy band diagrams of the metal and semiconductor in both non-contact and equilibrium conditions. For example, consider a lightly doped n-type semiconductor with a Φ_s and a metal with a Φ_m. If the Φ_m is higher than that of the Φ_s, and the metal and n-type semiconductor are isolated from each other, the energy levels in the semiconductor will remain constant, and their Fermi levels will become independent of each other.

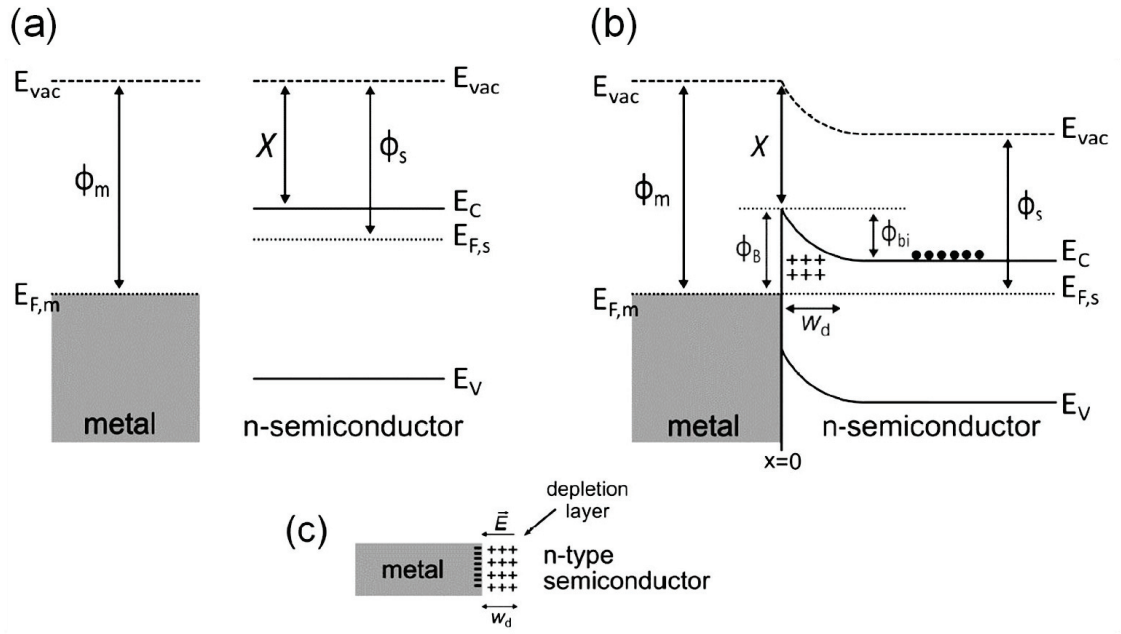


Figure 2.10. Energy band diagram of metal and n-type semiconductor (a) before and (b) after contact. The formation of the depletion layer can be seen in (c) (Adapted from Ref.[77])

In the case of our example, when the metal and n-type semiconductor are brought into intimate contact as shown in Figure 2.10 (b), the individual Fermi levels become aligned through charge transfer across the junction. This occurs because the electrons at the E_C^{sc} have higher energy than those of the metal, causing a transfer of electrons from the semiconductor to the metal until their Fermi levels become aligned, reaching equilibrium. As electrons move from the semiconductor to the metal, they leave behind holes, which generate an electric field at the junction, counterbalancing any further electron flow (as depicted in Figure 2.10 (c)). Here, the ionized donors in the n-doped semiconductor become immobilized as electrons diffuse to the metal, creating a depletion layer that extends over a distance within the semiconductor. When electrons flow from a semiconductor towards a metal, the electron concentration in the semiconductor decreases and the conduction band bends upwards. Due to the different work functions of the materials, a depletion region (W_d) is formed in the semiconductor, leading to a built-in potential (Φ_{bi}). This built-in potential can be defined as $\Phi_{bi}=\Phi_m-\Phi_s$, where Φ_m and Φ_{SC} represent the work functions of the metal and semiconductor, respectively. Essentially, the Φ_{bi} corresponds to the amount of band bending that occurs in the Si. In MS Schottky diodes, the Φ_B plays a crucial role by preventing electron flow from the metal into the semiconductor side. The Φ_B is determined by the Schottky-Mott model

which is defined as the difference between the Φ_m and the χ of the semiconductor and it is written as following [68].

$$\Phi_B = \Phi_m - \chi \quad (2.5)$$

According to the Schottky-Mott relation, the Φ_B is determined solely by the choice of metal used, and is not affected by the doping level of the semiconductor. In addition, the use of high Φ_m on n-type semiconductors has been shown to improve rectification, as this combination results in a larger Φ_B in the MS junction. Although the Schottky-Mott model can be used to estimate the Φ_B, it is important to note that the value obtained from this model may differ from the experimentally measured Φ_B value [78]. This is due to the fact that the model assumes an ideal case without any interface states or other anomalies such as a thin oxide layer or image force lowering at the junction interface [79-81].

Such non-ideal effects at the interface of MS junctions have been discussed in detail in the following section.

2.3.2. Non-ideal effects at the MS interface

Contrary to the Schottky-Mott relations in the ideal case, experiments have shown that the SBH is less sensitive to the Φ_m [78, 79]. This is due to the neglect of certain effects that take place at the interface between the metal and semiconductor. In reality, the semiconductor surface is not as smooth as predicted in theory, and may have surface states and incomplete covalent bonds that exist within the band gap. Additionally, there may be crystal defects present at the surface that originated from the fabrication steps. As a result, the contact between a metal and a semiconductor is not atomically tight, and these effects bring additional complexities that make it challenging to observe the physical phenomena of MS junctions. These surface states are distributed within the semiconductor bandgap and they affect the SBH due to the change in the charge distribution in the depletion region [69]. These phenomena have been extensively explained in the literature [68, 79].

One of the well-known non-ideal effects in MS junctions is Fermi level pinning, which has been extensively studied by J. Bardeen [82] to understand the effect of surface states on the Φ_B. This phenomenon is caused by the high density of surface states and is characterized by the neutral energy level (Φ_0) .When the Fermi level overlaps with the

Φ_0 at the surface, the net interface-trap charge will be zero, and as a result, the Fermi level at the junction is pinned by the surface states at Φ_0. This makes the Φ_B independent of the Φ_m. Another effect is the existence of a thin insulating layer at the MS interface. For instance, when Si is exposed to air, a native oxide layer that is less than 2 nm thick inevitably grows on its surface [83]. Figure 2.11 (a) shows a more realistic representation of the band structure of an MS Schottky contact that includes surface states and a thin insulator layer at the interface. This Φ_0 is located above the E_V separating acceptor and donor type surface states. The states above and below this Φ_0 correspond to acceptor-like and donor-like, respectively. The interface layer between MS contact induces the Φ_B by tunneling of charge carriers, which results in the increment of the Φ_B [68]. This increase provides better light sensitivity for MS Schottky PDs [82]. Therefore, a thin insulating layer between MS junction is deliberately employed to enhance the device characteristics.

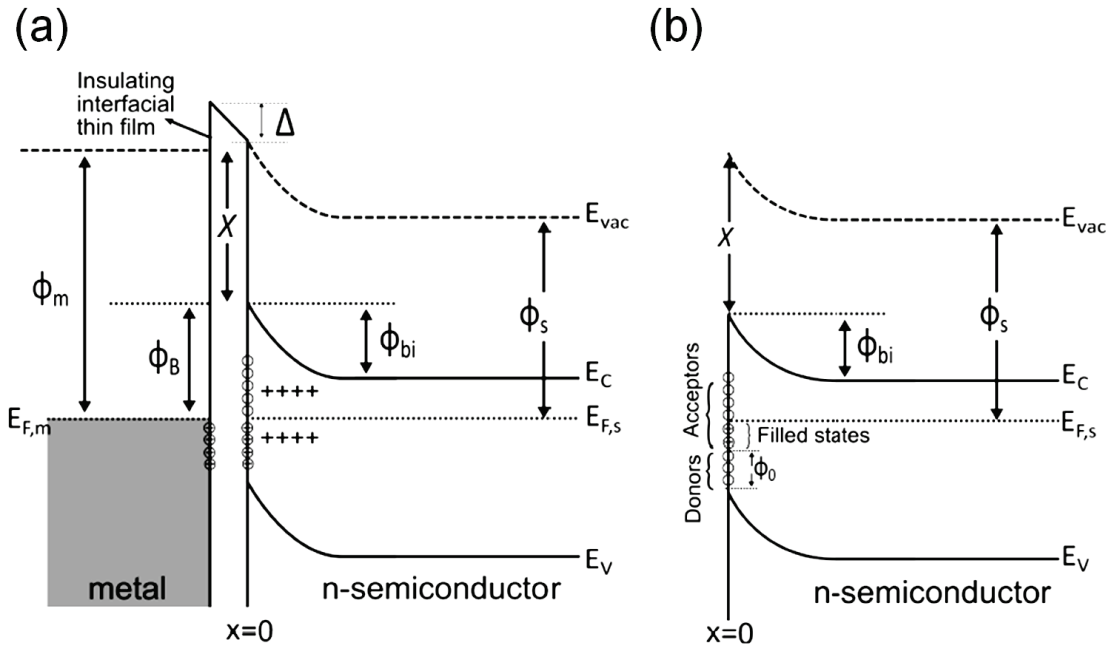


Figure 2.11. (a) Energy band diagram of a MS contact with a transparent atomically thin interfacial layer. Full and empty acceptor-like surface states are indicated at the interface. (b) Φ_0 separates the acceptor and donor type surface states (Source: Ref.[77])

Another effect predicted by the Schottky-Mott relation that causes a decrease in the SBH is Image force lowering. Here, the SBH is changed with the electric field occurs near the MS interface. Since the charge carriers are located close the MS interface, image

charges in metal are generated by these carriers and hence resultant potential decreases the SBH. The effect of image force lowering on the SBH of a MS junction has been extensively studied in the literature. Under different bias conditions, the application of a voltage changes the electrostatics at the interface, causing the barrier to become more rounded and reducing the SBH with increasing field [68]. However, it is important to note that the SBH can also be aligned depending on the bias voltage conditions due to the change in the depletion width at the junction. This effect of image force lowering makes the SBH a voltage-dependent parameter and is not related to the existence of an interfacial layer.

2.3.3. Current transport mechanisms in MS contacts

In a Schottky diode, the current is mostly carried by majority carriers, which are electrons in an n-type semiconductor and holes in a p-type semiconductor. This is because the MS interface forms a barrier that blocks the flow of minority carriers, i.e., holes in an n-type semiconductor and electrons in a p-type semiconductor. As a result, the Schottky diode exhibits low junction capacitance and fast recovery time compared to p-n junction diodes, where the current transport is controlled by both majority and minority carriers.

In a Schottky junction, the direction of current flow depends on the applied bias voltage. When a forward bias is applied, electrons flow from the semiconductor to the metal contact. In this non-equilibrium state, the fermi level of the semiconductor moves upwards, reducing the barrier height by the amount of the forward bias voltage. Conversely, under reverse bias, the barrier height increases by the amount of the reverse bias voltage, preventing electrons from flowing from the metal to the semiconductor. It's important to note that, in the absence of any anomalies, such as image-force lowering, the SBH remains constant in both forward and reverse bias conditions. This characteristic of the Schottky junction, where the current flow is mostly governed by majority carriers, results in a low junction capacitance and fast recovery time compared to p-n junctions, which rely on minority carrier transport. When a bias voltage is applied, the junction is said to be in a non-equilibrium state, causing the Fermi level of the semiconductor to move upward or downward. In the case of forward bias, the barrier is reduced by the amount of the forward bias voltage (qV_f) when the metal contact is positively biased

relative to the semiconductor. This reduction in barrier height allows electrons to move more easily from the semiconductor into the metal. Under reverse bias, the MS barrier is increased by the amount of the reverse bias voltage (qV_r), resulting in a larger barrier for electrons to overcome when flowing from the metal to the semiconductor. Therefore, the current flow in the reverse bias direction is strongly suppressed due to the Schottky barrier and SBH value is constant in both forward and reverse bias conditions, unless there are any anomalies such as image-force lowering.

Figure 2.12 shows five basic transport processes occurred at the junction of metal and n-type semiconductor under forward bias. Those processes are; (a) emission of electrons from the semiconductor over the top of the barrier into the metal. This process is known to be dominant for moderately doped semiconductors ($N_d < 10^{17}$ cm^{-3}) [68] at certain temperatures, (b) quantum-mechanical tunneling of electrons through the barrier which is critical for heavily doped semiconductors and responsible for ohmic contacts, (c) recombination of electrons and holes in the depletion region, like observed in a p-n junction, (d) electron diffusion in depletion region and (e) diffusion of holes injected from the metal into the semiconductor. The charge transport across a Schottky diode can be varied depending on the temperature and doping level of the semiconductor.

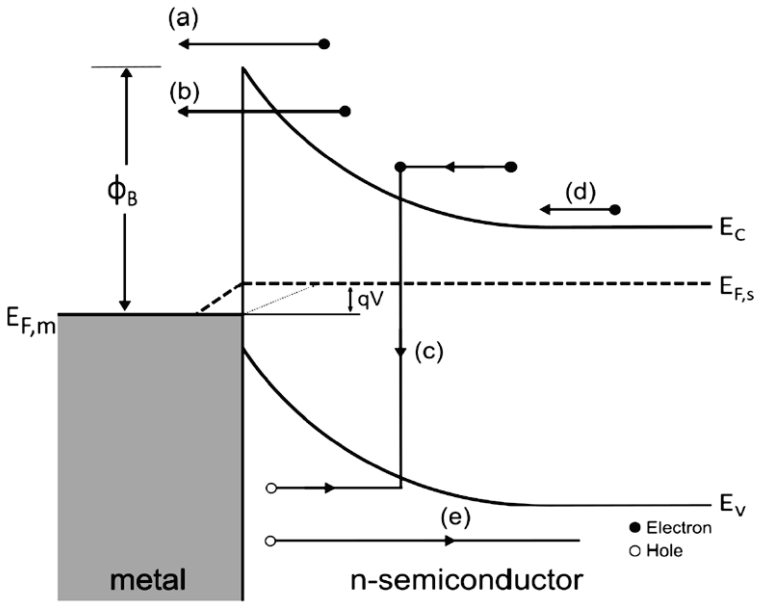


Figure 2.12. Transport mechanisms in the energy band diagram of M/n-Sc Schottky junction under forward bias (Taken from Ref.[77])

2.3.4. Thermionic emission and diffusion over the barrier

The thermionic emission (TE) theory and the diffusion theory are the two main theories that explain the charge transport mechanisms in Schottky diodes. The TE is applicable to high mobility semiconductors, where the transport of carriers is primarily governed by thermal energy. In the context of Schottky contacts, the TE theory refers to the transfer of carriers from the semiconductor to the metal or from the metal to the semiconductor over the potential barrier when the carriers gain sufficient thermal energy. Under forward bias, the applied voltage reduces the height of the barrier for electrons on the semiconductor side of the junction, allowing them to flow more easily from the semiconductor into the metal. This results in an increase in current from the semiconductor to the metal. However, under reverse bias, the applied voltage increases the height of the barrier for electrons on the semiconductor side, making it more difficult for them to flow from the metal to the semiconductor. This results in a decrease in current from the metal to the semiconductor. The majority charge carriers which are usually electrons are responsible for this current flow in Schottky diodes. The TE assumes that the barrier height of the system is much higher than the thermal energy of the system, which is on the order of *kT/q*. This theory also assumes that the system is in thermal equilibrium at the interface and that the thermal equilibrium of the system is not affected by charge accumulation at the interface [75]. The current density can be written as indicated below;

$$J_{sm} = A^{*}T^{2}exp\left(\frac{-q\,\Phi_B}{k_BT}\right)exp\left(\frac{qV}{k_BT}\right) \qquad 2.6$$

where q, T, k_B are the elementary charge, the absolute temperature, the Boltzmann constant, respectively. A^{*} is known as the effective Richardson constant (~112 $Acm^{-2}K^{-2}$ for n-Si [84]). From this, one can calculate the effective barrier height and ɳ of junction [85]. It should be considered that the Richardson constant, which is formulized as $A^{*} = 4\pi qm^{*}k^{2}/h^{3}$, is principally an intrinsic property of a semiconductor and depends on the effective mass carriers (m^{*}) at conduction band edge. In addition, some factors that cause non-ideal conditions such as inhomogeneities in the Schottky barrier, interfacial layers and tunneling of charge carrier can vary the value of A^{*} [86].

Since the SBH is independent of applied bias voltage, the current density from metal to semiconductor remains constant. Therefore, J_{ms} is given by,

$$J_{ms} = -A^{*}T^{2}exp\left(\frac{-q\,\Phi_B}{k_BT}\right) \quad 2.7$$

then, the total current density is written by the sum of equations 2.6 and 2.7,

$$J = A^{*}T^{2}\left[exp\left(\frac{-q\,\Phi_B}{k_BT}\right)exp\left(\frac{qV}{k_BT}-1\right)\right] \quad 2.8$$

$$= J_s\left[exp\left(\frac{qV}{k_BT}-1\right)\right] \quad 2.9$$

where J_s is the saturation current density. It is obvious that J_s depicts exponentially dependent on SBH and inversely proportional to temperature.

In contrast to ideal Schottky contact, current transport deviates from the TE behavior described in equation 2.9. In practical Schottky diodes, TE model of non-ideal junctions can be expressed as in the following,

$$J = J_s\left[exp\left(\frac{qV}{\eta k_BT}-1\right)\right] \quad 2.10$$

where η of the diode is defined as a measure how closely the diodes follows an ideal diode equation. Moreover, the important Schottky diodes parameters such as SBH, sheet resistance (R_s) and η can be derived from the slope (or intercept) of linear region of the equation 2.10.

The diffusion theory suggests that the current in a Schottky diode is limited by both the drift (local electric field) and diffusion (carrier concentration gradient) processes in the depletion region [87]. According to this theory, the electrons are in thermal equilibrium with the lattice even when the junction is forward biased, and their quasi-Fermi level coincides with the Fermi level at the interface (as shown in Figure 2.12 by the dotted curve). However, in a subsequent work, Bethe [75] assumed that the effect of the diffusion process in the depletion region is negligible, and the current flow is restricted by both the transport of electrons through the space charge region and the TE over the barrier [87]. It should be noted that the validity of both theories depends on various factors such as the doping concentration, the temperature, and the geometry of the diode.

In the tunneling mechanism, the charge transport across the barrier is dominated by quantum mechanical tunneling, particularly in heavily doped semiconductors or at low temperatures. It allows charge carriers to be transported from the semiconductor to the

metal or vice versa, bypassing the potential barrier through a process that violates classical mechanics [69]. The tunneling probability depends on the barrier height, width, and the effective mass of the carriers, and can significantly affect the behavior of Schottky diodes. The importance of tunneling current in the total current flowing across the junction is dependent on the doping level and temperature of the semiconductor. In heavily doped semiconductors and/or at low temperatures, the transport may be dominated by the tunneling current [68, 69]. This means that charge carriers can tunnel quantum mechanically from the semiconductor to the metal or vice versa.

Figure 2.13 (a) and (b) schematically show the tunneling process for forward and reverse biases respectively. In the case of heavily doped semiconductors, the Fermi level is positioned above the bottom of the conduction band, and the tunneling process is known as field emission (FE). At higher temperatures, a considerable number of electrons occupy energy states above the Fermi level, where the potential barrier is thinner and lower. These thermally excited electrons can tunnel the barrier by a mechanism known as thermionic field emission (TFE). The heavily doped semiconductor has a very narrow depletion region, which allows for the Fermi level to be above the bottom of the conduction band. This creates a situation where the tunneling process is dominated by the FE mechanism. At higher temperatures, the thermal energy of the electrons allows them to populate energy states above the Fermi level, which reduces the effective height of the tunneling barrier. This can lead to a significant increase in the tunneling current, which is referred to as TFE.

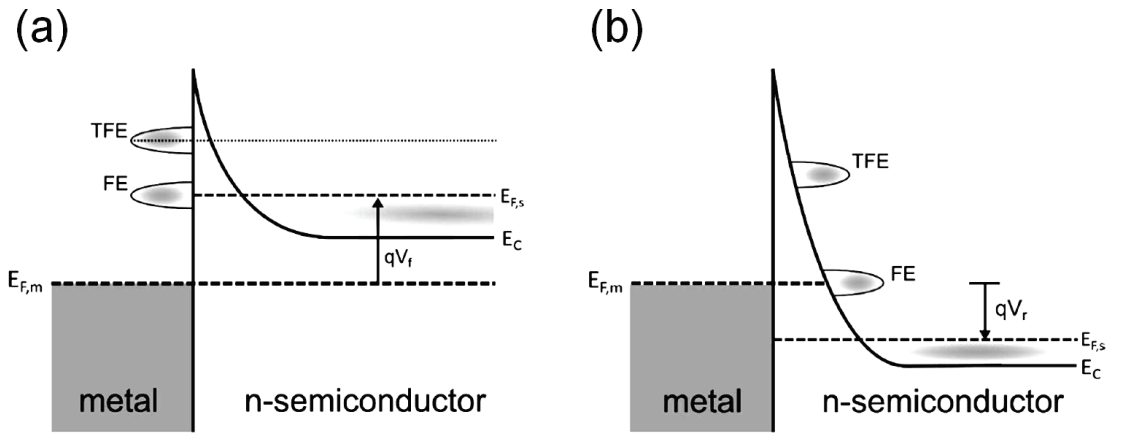


Figure 2.13. The energy band diagram of a Schottky contact constructed on a highly doped n-type semiconductor can be used to qualitatively illustrate the FE and TFE tunneling currents under (a) forward bias and (b) reverse bias, respectively. (Adapted from Ref.[77])

2.4. Measurement of Schottky barrier height

At zero bias, the Fermi level of the metal and the semiconductor are at the same energy level. In this case, only the TE of majority carriers governs the current flow across the junction. For a Φ_m is greater than E_C^{sc}, the potential barrier is too high for TE of electrons from the semiconductor to the metal. Therefore, there is no net current flow across the junction under zero bias conditions. Therefore, the total current across the junction where the J_{sm} and J_{ms} is given by,

$$J_{ms} + J_{sm} = 0 \tag{2.11}$$

As J_{sm} was expressed by the equation 2.6 earlier, J_{ms}, referred by reverse saturation current ($-J_{sm}$) can be written as below,

$$J_{sm} = A^* T^2 exp\left(\frac{-q\,\Phi_B}{k_B T}\right) \tag{2.12}$$

The Shockley equation is derived based on assumptions such as TE being the dominant charge transport mechanism and the depletion region being much smaller than the device dimensions. It is related with the current flowing through a Schottky diode to the applied bias voltage and other device parameters such as η and the SBH and can be expressed as [68],

$$J = J_{ms} + J_{sm} = J_0 \left[exp\left(\frac{q(V - IR_s)}{\eta k_B T}\right) - 1\right] \tag{2.13}$$

where, J_0 and IR_s are the reverse saturation current density and the voltage drop due to the R_s, respectively. Based on TE theory, the I–V relation for a Schottky diode under the forward bias should be a value of qV > 3kT [88] for the equation 2.13. Here, η represents the degree of TE at the interface which is generally used to measure the deviation of practical diodes from the ideal condition where η = 1. The major diode parameters of MS Schottky contacts such as Φ_B, η and R_S can be determined using I-V characterization of diode under dark conditions. A representation of absolute value of the I-V curve for MS contact in dark conditions was shown in Figure 2.14 (a). Moreover, the important Schottky diodes parameters such as Φ_B, R_s and η can be derived from the slope (or intercept) of linear region of forward bias region in I-V plot.

The MS contact exhibits characteristic diode behavior, where the current conduction is higher in the forward bias region and lower in the reverse bias region. From forward bias region of I-V plot, the Φ_B, η and R_S can be extracted using the method developed by Cheung [89]. In the case of forward bias with high enough values, the -1 term in the equation 2.13 can be neglected, so the equation yields in term of voltage as,

$$V = \frac{\eta k_B T}{q} ln\left(\frac{I}{I_0}\right) + IR_s \qquad 2.14$$

taking the derivative of equation 2.14 with respect to I,

$$\frac{dV}{dlnI} = \frac{\eta k_B T}{q} + IR_s \qquad 2.15$$

the equation 2.15 can be obtained. It should be noted that *dV/dlnI* versus *I* plot generates a straight line and the R_S value of diode is found from slope of this plot. As figured out in Figure 2.14 (b), the η can be also extracted as $\eta k_B T/q$ from the intercept of this line in the same plot. Thus, η of the diode can be calculated as following.

$$\eta = \frac{q}{k_B T} \frac{dV}{dln(I)} \qquad 2.16$$

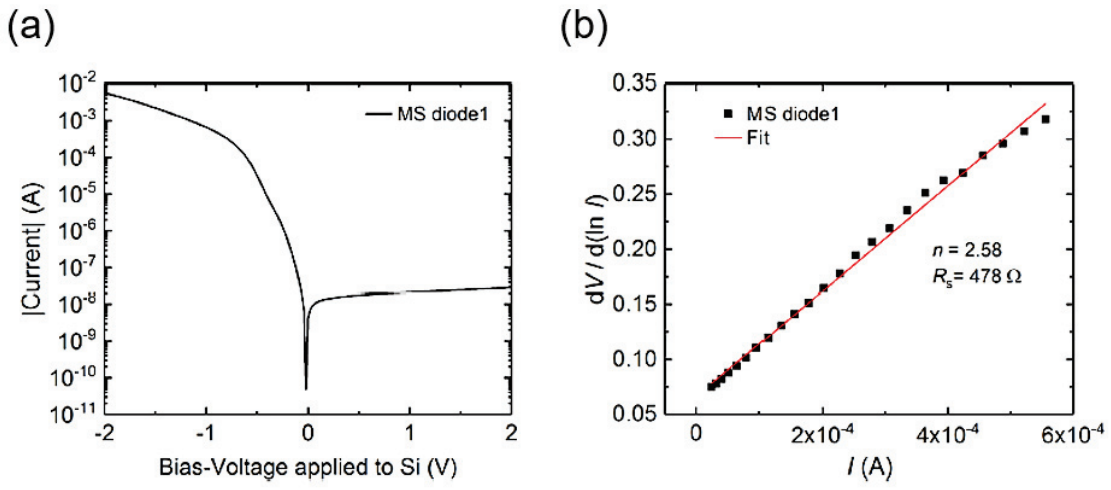


Figure 2.14. (a) Semi-logarithmic plot of a representative MS diode in dark conditions. (b) dV /dlnI vs I plot to extract the diode parameters according to Cheung`s method. (Adapted from Ref.[77])

Furthermore, in order to estimate the Φ_B of the MS junction, the following function of $H(I)$ can be defined from the equation 2.14.

$$H(I) = V - \frac{\eta k_B T}{q} \ln\left(\frac{I}{AA^* T^2}\right) = IR_s + \eta\Phi_B \qquad 2.17$$

Here, A is the active junction area of the diode in a unit of cm^2. The Φ_B can be determined from the intercept of the linear region of $H(I)$ vs I plot.

2.5. Working principle of Schottky barrier photodetectors

In a PD, when light strikes the junction, photons with energy equal to or greater than the bandgap energy of the semiconductor are absorbed, generating excess electron-hole pairs that are separated by the electric field in the depletion region. The position of the depletion region significantly impacts the spectral R of the PD since it is affected by the penetration depth, which varies with wavelength $(1/\alpha)$. Schottky PDs are known for their high efficiency as PDs due to their ability to operate much faster and more efficiently than p-n junction PDs [90]. The formation of the depletion region in Schottky junctions occurs at the MS interface, which is determined by the energy difference between the Φ_m and the semiconductor's χ. The depletion region forms underneath the semiconductor surface in Schottky junctions, whereas it is buried inside the semiconductor in p-n junctions.

Unlike typical p-n PD, Schottky PDs require a transparent metal contact in order to allow the light to enter the semiconductor material. Schottky junction PDs can operate in two modes: i) when a reverse bias is applied, it is known as photoconductive mode ii) when there is no bias voltage, it is named as photovoltaic mode. Higher photocurrent may be achieved from the diode in photoconductive mode because applying reverse bias causes the width of depletion region to be widen. As more photons penetrates to the widen depletion region, the amount of photogenerated charges increases and hence, photocurrent increases. However, this mode causes the increment in dark current noise which decreases the detector sensitivity. When operating in photovoltaic mode, a Schottky PD generates charge carriers solely through exposure to light, resulting in limited photocurrent due to the charge carriers being created only within the depletion region, but this mode does not require an external power source. Additionally, Schottky PDs are highly efficient PDs, offering faster and more efficient performance compared to other types of PDs [90].

Figure 2.15 illustrates the schematic of absorption process and photo-carrier separation in Schottky junction PDs with its corresponding energy band diagram. The photogenerated charge carriers within the depletion region undergo rapid separation due to the strong built-in electric field and subsequently migrate towards the electrodes, where they are efficiently collected. Nonetheless, charges generated in the neutral regions must undergo diffusion into the depletion region to actively contribute to the photocurrent. In order to expose the semiconductor to light, a thin metal contact (less than 10 nm) contact is necessary in Schottky PDs, which distinguishes them from p-n PD. Here, the thickness of this deposited thin metal layer limits the amount of absorbed light by the underlying semiconductor. As will be demonstrated later in the sections of 2.6 and 2.7, the highest possible light transmission into the semiconductor is made feasible by using graphene as a transparent metal contact in Schottky junctions.

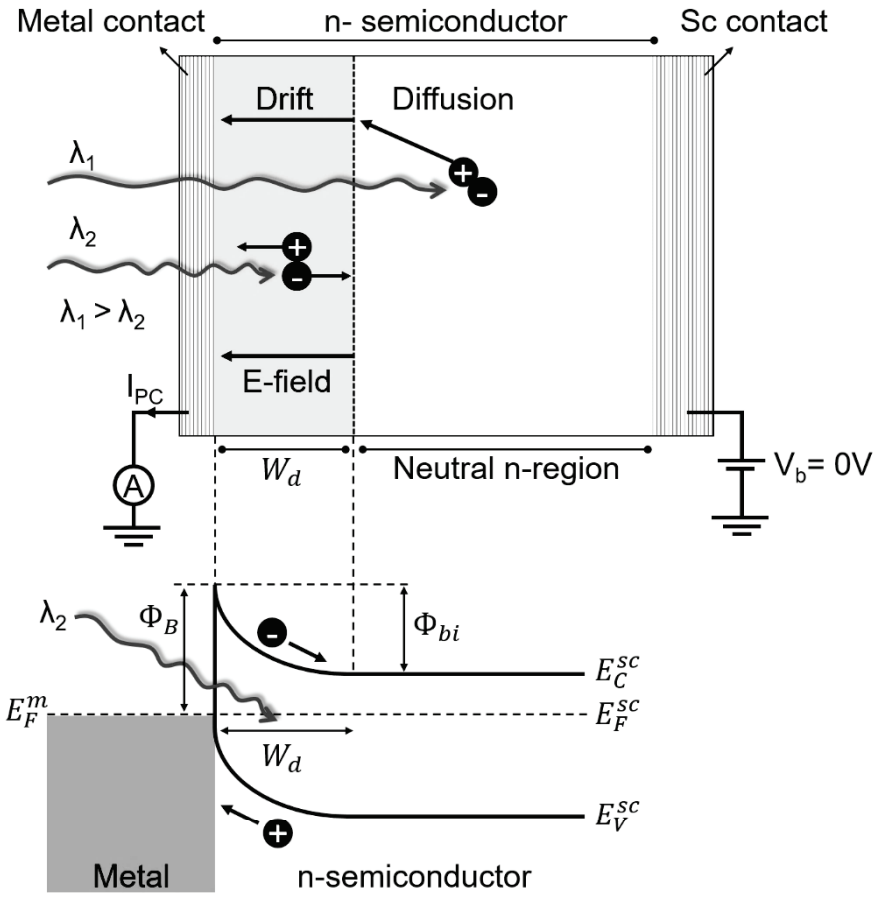


Figure 2.15. Energy band diagram of a typical metal/n-type semiconductor Schottky junction at zero bias and under light illumination The incident light is remarked to illustrate the wavelength-dependent penetration depth and image is redrawn from Ref.[77].

2.6. Graphene/semiconductor Schottky junction

Graphene is a promising material for TCEs in MS Schottky devices due to its exceptional electrical and optical properties, including high carrier mobility and transparency. In contrast to the MS interface where the Fermi level of the metal remains constant due to its high density of states, graphene has linear dispersion relation at the Dirac point results in a semi-metallic (or zero-gap semiconductor) nature. As a result, even a small change in charge carrier density can have a significant impact on the Fermi level of graphene. This section will delve into the characteristics of graphene/semiconductor (G/Sc) Schottky junctions.

G/Sc junctions have gained significant interest as a replacement for MS junction in Schottky diodes. In these junctions, a potential energy barrier is formed at the interface, similar to MS junctions. However, unlike conventional junctions, the SBH in G/Sc junctions can be tuned by modifying the work function of graphene (Φ_G) through various methods such as chemical doping, temperature, desorption/adsorption of atmospheric adsorbates, and electrostatic gating. This alteration in Φ_G allows for the potential barrier height to be changed as a function of applied bias. Similar to conventional junctions, the majority carrier of the semiconductor plays a critical role in determining the rectifying or ohmic character of the G/Sc junction.

The G/Sc heterojunction exhibits strong rectification and can be used in Schottky barrier devices such as tunneling field-effect transistors and low-leakage current PDs. Studies have shown that G/Sc heterojunction devices show a rectification behavior when CVD-grown graphene is transferred onto conventional semiconductor materials like Si, GaAs, SiC, and GaN. SBH values can be extracted from the Arrhenius plot (J-V) of various G/Sc junctions and found to be 0.86, 0.79, 0.91, and 0.73 eV for Si, GaAs, SiC, and GaN junctions, respectively [7]. The Fermi level of graphene in such G/Sc heterojunctions varies with the applied bias voltage due to charge transfer at the interface, which modifies the Φ_G and leads to the variation of the SBH. Tongay et al. proposed a modification to the TE theory that accounts for the variation of the Fermi level in graphene [91]. This modification helps to explain the increase in the reverse saturation current observed in G/Sc junctions with increasing bias voltage. As a result of the high density of states in the metal, the charges induced in the metal by the semiconductor are negligible in a MS interface, but the effect of induced charges is instead no longer

negligible for graphene as mentioned above. Figure 2.16 shows the energy band diagram of graphene/n-type semiconductor (G/n-Sc) Schottky junction at zero bias, under forward and reverse bias conditions. The Fermi level of graphene is assumed at the at the Dirac point when there is no applied bias. As seen in Figure 2.16 (a), when graphene contacts with a lightly doped n-type semiconductor, At the interface of G/Sc, the SBH and depletion region are formed until the junction reaches thermal equilibrium. The depletion region inside the n-type semiconductor fills with holes, and an equal number of electrons are induced in graphene in thermal equilibrium. Under forward bias, the Fermi level of graphene shifts downwards because fewer charges are needed to transmit positive charges formed in the depletion layer of the semiconductor (as shown in Figure 2.16 (b)). This causes the width of the depletion region of the junction to decrease, and the SBH increases proportionally with the decrement in the Fermi level of graphene. On the other hand, under reverse bias (Figure 2.16 (c)), the depletion layer in the semiconductor increases, and the number of negative charges in the graphene also increases, causing the Fermi level to shift upwards through the Dirac point. This leads to a decrease in the SBH and an increase in the depletion region.

Since the main focus of this thesis is on graphene/n-type silicon (G/n-Si) Schottky junction PDAs, a more detail related to such diodes is given in the section of 2.7.

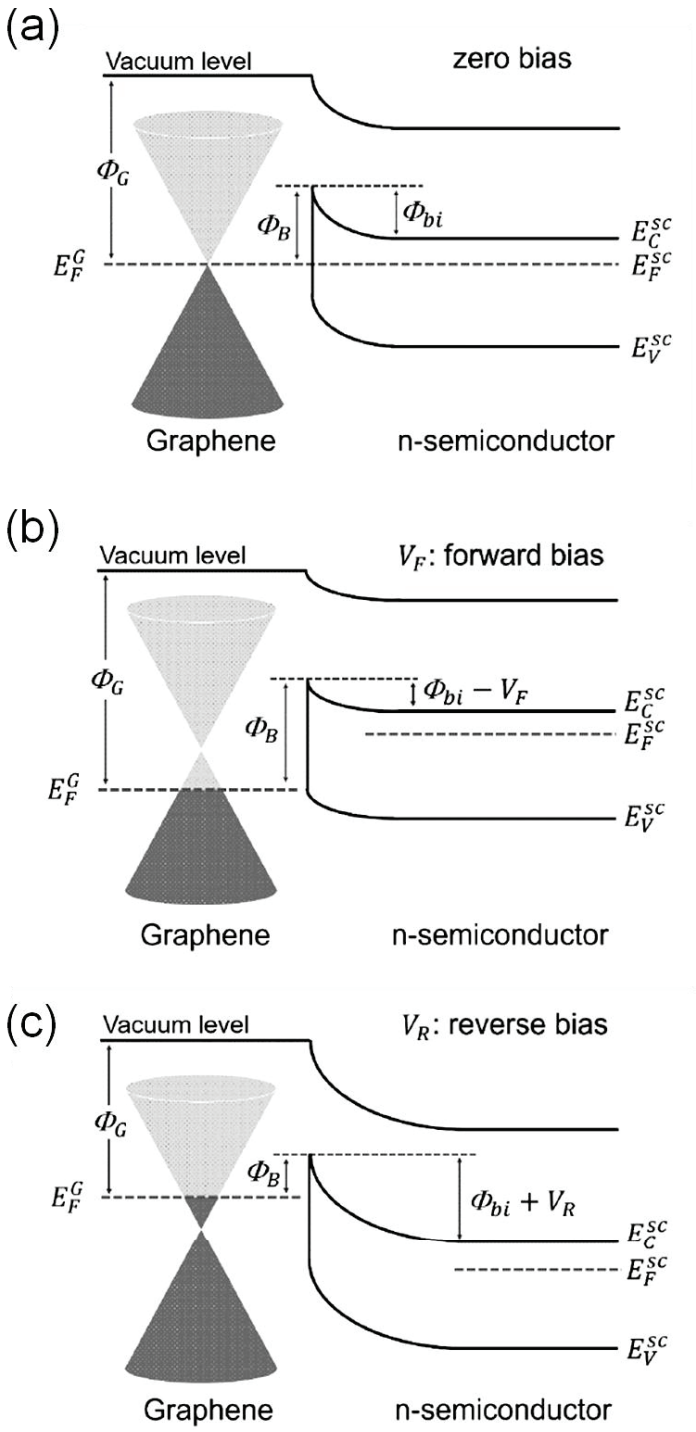


Figure 2.16. Energy band diagram of a graphene/n-type semiconductor Schottky junction (a) at zero bias, under (b) forward and (b) reverse bias voltages. (Source: [92])

There are several key performance parameters used to characterize the effectiveness of graphene-based PDs, including *R*, signal-to-noise ratio (*S/N*), specific detectivity (D^*), noise-equivalent power (*NEP*), and response speed.

The *R* is one of the most crucial diode parameters to characterize the light sensing properties of diodes and is defined as the ratio of generated photocurrent (I_p) to the

incident light power (P) at a certain wavelength (in a unit of ampere per watt, A/W) and is expressed by the formula below,

$$R(A/W) = \frac{I_p - I_d}{P} \tag{2.18}$$

where I_d is the dark current. In other words, R is a measure of the conversion of the light power into photocurrent. The magnitude of R is dependent on the wavelength of the incident light. Moreover, the application of reverse bias voltage causes a slight increase in the R value owing to the improved depletion region of the PD.

The S/N is important parameter to determine minimum detectable signal strength. One of the main factor contributing to the total noise is the dark current in PDs [68] and S/N can be described as follows.

$$S/N = \frac{Signal\ Power}{Noise\ Power} \tag{2.19}$$

By using the measured R values of the diodes, the D^* and NEP of the devices can be calculated through equations 2.20 and 2.21, respectively. D^* represents the minimum detectable level of light by the PD, with a device junction area of 1 cm^2 and can be determined by,

$$D^* = \frac{A^{1/2}R}{\sqrt{2qI_d}} \tag{2.20}$$

where, q and A are the elementary charge and the active junction (photosensitive) area of the diode, respectively. The unit of D^* is $cmHz^{1/2}W^{-1}$ and named as ″Jones″. D^* is a key parameter in evaluating the performance of a PD, which is determined by the detector's sensitivity, spectral response, and noise. It represents the lowest level of light that can be detected by the PD for a given signal-to-noise ratio. D^*, which is determined by the detector's active area, is commonly used to compare the sensitivity limits of different PDs.

Furthermore, NEP corresponds to the incident power required to obtain a S/N of 1 at a bandwidth of 1 Hz and is defined as following,

$$NEP = \frac{A^{1/2}}{D^*} = \frac{\sqrt{2qI_d}}{R} \tag{2.21}$$

NEP is expressed in a unit of $WHz^{-1/2}$. If the active area of device is decreased, then the noise of a PD also reduces as seen from the equation 2.21. Also, it can be referred to be reciprocal of D^*, normalized with respect to the junction area. A smaller NEP value indicates a more sensitive PD, while a high value of D^* yields greater sensitivity. Therefore, achieving a better PD performance corresponds to having a lower NEP value.

The response speed of a PD can be used as the response of a photocurrent to an optical signal is characterized by the rise/decay times, defined as the times at 10% to 90% of their maximum photocurrent values, respectively. These properties are closely linked to the charge transport and collection mechanisms as well as the bandwidth of the device's photoresponse.

2.7. Graphene/silicon based Schottky junction photodetectors

A graphene/silicon (GSi) Schottky PD can be created by combining graphene with lightly doped n-type Si (n-Si) substrate. In this device, graphene serves as a TCE due to its approximately 2.3% optical absorption and Si is used as light absorbing material as mentioned before. Here, high optical transmittance of graphene enables detection of radiation with energies above the Si band gap [93] and the spectral response of the PD is dependent on the band gap of Si which corresponds to the visible and short-wavelength infrared spectral range in electromagnetic (EM) spectrum.

GSi based Schottky junction PD fabrication and performance enhancement have been the subject of numerous studies. In one study, Riazimehr et al. fabricated G/n-Si PD on n-type Si wafers (~ 500 μm) with a thermally deposited SiO_2 layer of 85 nm. In this work, they revealed the Schottky rectifying behavior of the junction occurred by p-type CVD graphene on Si substrate [94]. Figure 2.17 (a) and (b) shows a schematic diagram and color enhanced SEM image of the fabricated device, respectively. In the device design, G is in contact with a Cr/Au pad on SiO_2 side forming an ohmic contact and lies on n-Si surface without touching the Cr/Au pad located on n-Si side. The surface where G and n-Si meets is called as the active area of the Schottky junction and plays a crucial role in the device performance [95]. The J-V characteristic of this diode in dark and under illumination can be seen in Figure 2.17 (c) and (d). These results show that the fabricated device exhibits a clear rectifying behavior and the photocurrent (I_{PC}) based on light illumination can be observed due to the increment in the current value at V_b = 0V as

remarked from the J-V curve plotted in semi-logarithmic scale. In addition, the voltage difference points out the open-circuit voltage (V_{OC}) in horizontal scale.

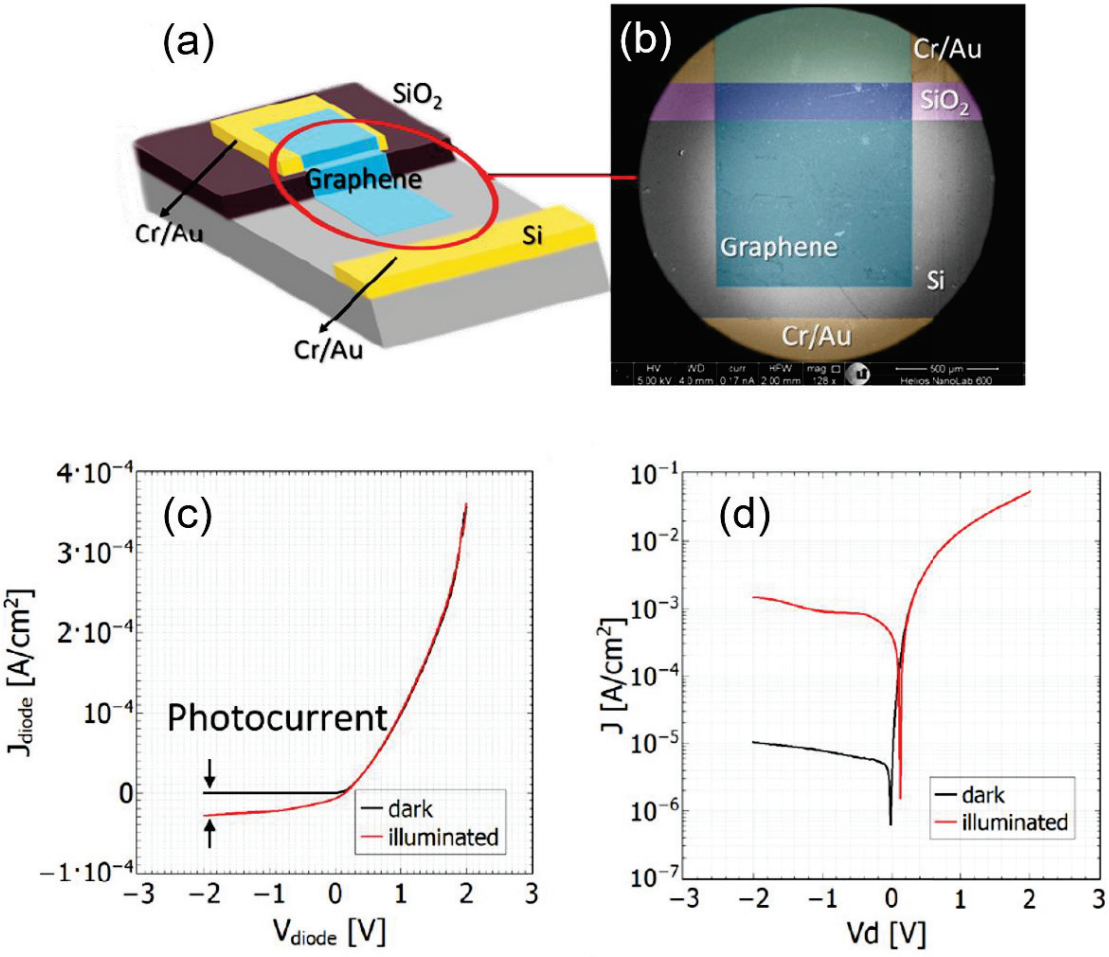


Figure 2.17. (a) Schematic and scanning electron micrograph of a graphene PD. The color enhanced SEM image shows the exact position of the graphene, SiO_2, and metal electrodes. J-V plot of the G/n-Si diode on (b) linear and (c) semi-logarithmic scale in the dark and (d) under illumination, respectively (Adapted from Ref.[94])

Overall, the GSi Schottky diode offers several advantages such as its simple architecture, large photoactive area, and potential for integration into CMOS processing [96]. However, the device characteristics such as η, level of dark current, and spectral dependent photoresponse can be influenced by several factors such as interface properties, choice of materials, fabrication route, interfacial oxide layer, and graphene doping. Previously these factors have extensively investigated to understand their effects on device performances [10, 97, 98]. To date, the performance of GSi PDs in terms of response

speed remains far below that of Metal-Graphene-Metal (MGM) and commercial Si PDs which exhibit cut-off frequencies (f_c) on the order of GHz for free space light detection [99]. On the contrary to MGM and commercial Si PDs, GSi PDs have demonstrated response speeds on the order of 10s-100s of kHz for wavelengths above 500 nm. [100, 101]. This limitation can be attributed to speed-limiting diffusion currents due to photogenerated carriers deep within the bulk Si substrate (~500 μm) [12]. Additionally, owing to the diffusion current in the Si substrate and a large parasitic capacitance, their *R* and bandwidth are very limited [102]. These drawbacks lead to replace the GSi devices commonly employed bulk Si with SOI substrate and discuss the influence of active Si layer on SOI substrate on optoelectronic characteristics of the diode. Selvi et al.[12] revealed the Schottky rectifying behavior of the junction occurred by transferring graphene on a SOI with an active Si layer of 10 μm and less. The schematics of the devices can be seen in Figure 2.18 (a). The device structure contains 100 nm of amorphous silicon nitride (SiN_x) as an insulating layer to hinder the leakage from Gr contact to n-Si active layer. Here, electrical contact to G (Gr contact) and n-Si (Si contact) consist of Cr/Au (3 nm/50 nm) and Al/Cr/Au (50 nm/3 nm/50 nm), respectively. Figure 2.18 (b) represents the spectral response measurements of the PDs fabricated on SOI and bulk n-type Si with identical doping level. According to the measurements taken in a wide range wavelength from 400 nm to 1050 nm, the maximum R values shift towards lower wavelengths due to the decrement in the active Si layer thickness. This is related with the penetration of light through the PD. In SOI based devices, BOX and handle Si layer act as damping layers for the transmitted light and they can not contribute the photoresponse. That is the reason for the reduced *R* of the GSOI devices compared to G/n-Si devices fabricated on bulk Si for longer wavelength light $\lambda > 900$ nm. The high-speed optical response results of GSOI devices operated under self-powered conditions can be seen in Figure 2.18 (c). This measurement has been taken in the UV to NIR wavelengths range employing a picosecond (ps) white light laser source with a pulse duration of less than 80 ps and optical bandpass filters with a FWHM of < 10 nm. It can be seen that the rise- and decay-times of the both devices are in the range of nanoseconds (ns) and the variation in these results is related the difference in the active area of the junction in devices. According to this study, using a SOI substrate with an active Si layer thickness of 10 μm or less can greatly enhance the speed of GSi Schottky PDs while only slightly reducing their *R* compared to bulk Si counterparts.

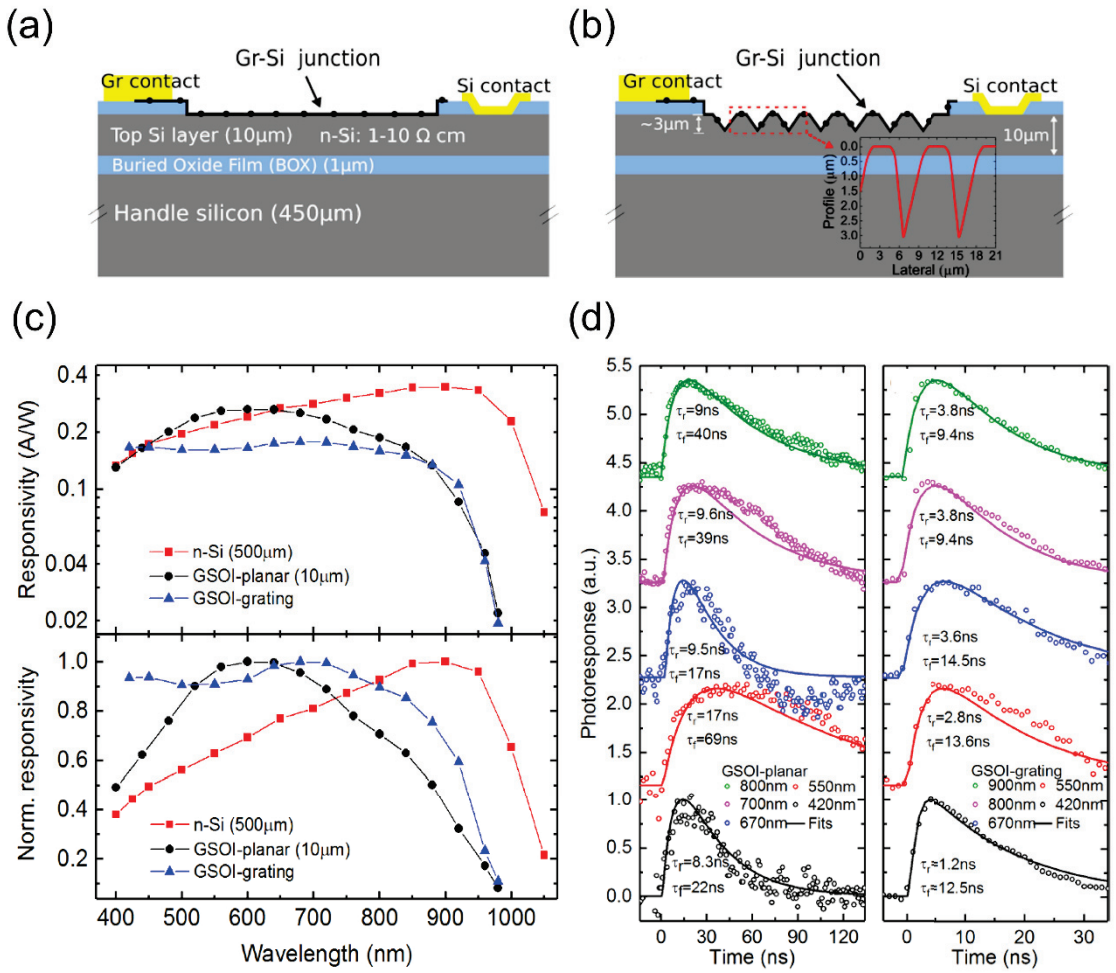


Figure 2.18. (a) Schematic structure of the GSOI-planar device where graphene is transferred on the planar Si surface and GSOI-grating device where graphene is transferred on the structured Si surface (b) Spectral and normalized responsivities of GSi Schottky PDs fabricated on SOI as planar and grating design and bulk Si. (c) Time-resolved photoresponse of the GSOI-planar and the GSOI-grating device under illumination with a picosecond white light source at various wavelengths under photovoltaic mode, respectively. (Adapted from Ref.[12])

Considering this work, SOI has numerous benefits in terms of complete dielectric isolation between neighboring devices, resulting in lower leakage currents and reducing capacitive coupling. Additionally, the active Si layer can be fully depleted, further improving device performance.

CHAPTER 3

FABRICATION AND CHARACTERIZATION

This chapter provides the details of the techniques and equipment used in the device fabrication and characterization. Fabrication of the devices was performed using the clean room facilities in Ermaksan Optoelectronic R&D Center in Turkey. Optoelectronic characterizations of the fabricated PDAs were carried out in the Quantum Device Laboratory (QDL) at the Physics department of Izmir Institute of Technology by conducting current-voltage (I-V), *R*, optical crosstalk and time dependent photocurrent measurements. In addition to determine the number of graphene layers and their uniformity single-point Raman spectroscopy and Raman mapping measurements were done in Katip Çelebi University Central Research Laboratory.

3.1. Fabrication of the devices

Graphene/n-Si Schottky PDAs were fabricated using standard photolithography and lift-off processes. A typical device fabrication process consists of various consecutive steps including preparation of the device patterning growth and transfer of graphene onto these patterned SOI substrates. Separate photolithography steps are then performed in the order allowing the n-Si array patterning, selective metal contact deposition, patterned graphene by O_2 plasma etching and removal of materials on the substrate.

3.1.1. SOI substrate preparation

A SOI wafer with a diameter of 6″ was purchased from Siegert Wafer, Germany and used for the fabrication of the PDAs. For the experiments, the substrates with sizes of around 10 mm × 10 mm are cleaved from the wafer using a dicer in METU MEMS Center. The SOI substrates consist of 10 μm thick n-doped photo-active silicon (Si (100)) (specification ρ = 1–5 Ω.cm, nominal doping level $N_d \approx 2 \times 10^{15}$ cm^{-3}), a thick BOX layer and thick substrate. Prior to fabrication procedures, the substrates are subjected to a multi-step cleaning process in order to remove possible contamination on the surface such as

hydrocarbon and particulate residues. The cleaning process consists of ultrasonic cleaning in acetone and isopropyl alcohol (IPA) for ten minutes each without letting the substrate dry while being transferred between solvents. Then, substrates are dried with a N_2 and become ready for device fabrication.

3.1.2. Photolithography

The device structures were prepared by using photolithography technique. In the fabrication route, different lithography steps were used to prepare 1D and 2D PDA device structures. Photolithography is based on defining geometric patterns in a layer of photosensitive material called photoresist. A typical photolithography process involves three main steps: photoresist (PR) spray or spin, exposure of the pattern and developing. There are two main types of PR: positive tone resists and negative tone resists (Figure 3.1). In positive tone resists, the regions exposed to UV radiation become soluble and can be removed in a developer solution; whereas in negative tone resists, the exposed regions become insoluble and resistant to developers.

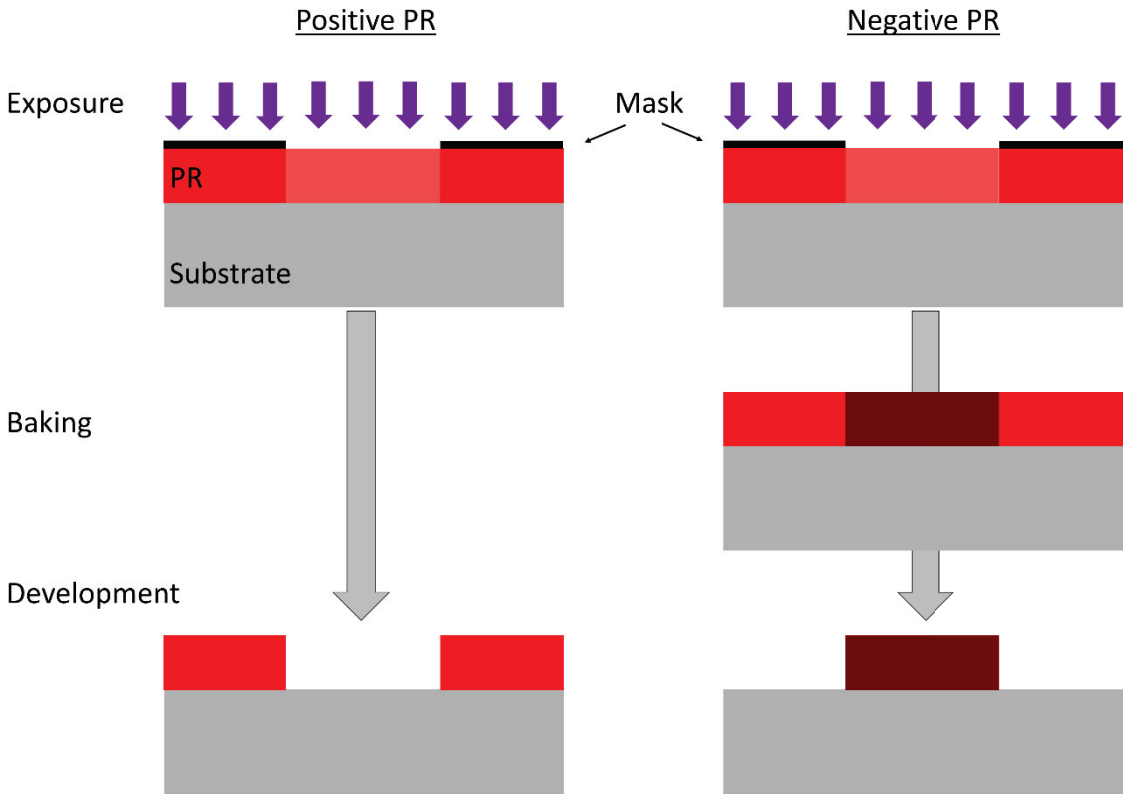


Figure 3.1. Photolithography processes using positive tone and negative tone PR.

Image reversal is a process to reverse the tone of positive photoresists. Similar to a negative photoresist, areas that are exposed become “protected”, while the unexposed areas will be developed away. With the additional process steps “reversal bake” after image-wise exposure and subsequent “flood exposure”, the material provides a negative resist image which is characterized by a particularly high contrast of patterns. As a recommended guideline value for the reversal bake, samples are baked at 115 °C during 20 min on a hot plate at 115 °C. The subsequent flood exposure (2- to 3-fold exposure dose of the initial exposure) converts the unexposed areas into a developable form. For optimal patterning, the process steps image-wise exposure, flood exposure, and development have to be coordinated thoroughly (see Figure 3.2).

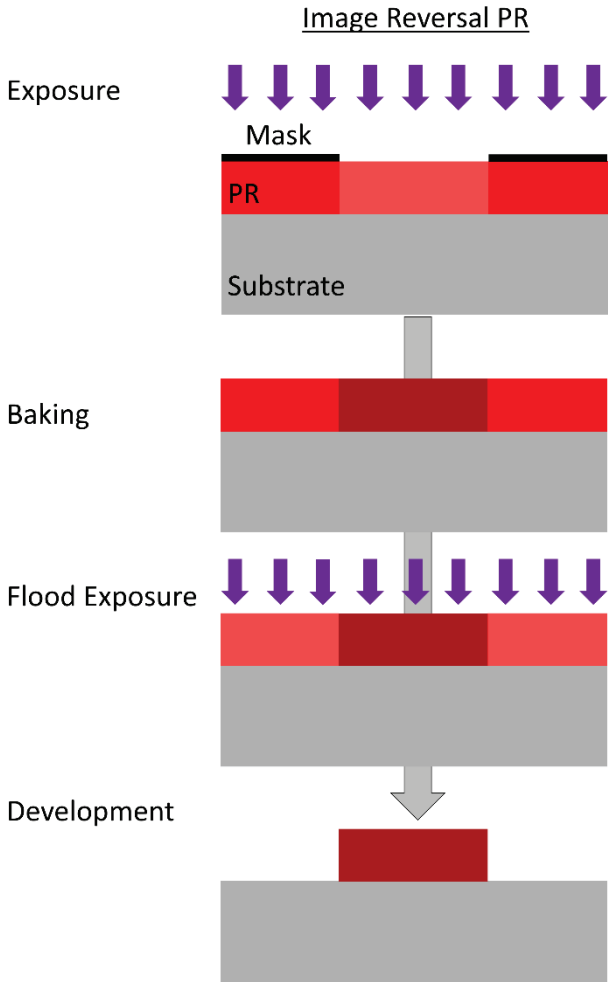


Figure 3.2. The schematic representation of image reversal process.

The thickness of the resist film depends on the choice of concentration of PR, applied spin speed and spray duration. In our study, we used two different resist coating systems called as spray and spin coater. Thick PR was laid on SOI substrate with a spray

coater system to pattern n-Si arrays in order to make the photoresist robust to plasma in media, but thin PR was coated on substrate by using spin coater system to pattern graphene layers and metal contact areas on substrate. Throughout this work, AZ5214E and TI35E series positive PR and AZ726 MIF as developer (Microchemicals GmbH) were employed in the photolithography processes. The optimized resist thicknesses for AZ5214E and TI35E were given in detail in the schematics of fabrication routes of devices in the sections of chapter 4. Here, AZ5214E resist was used to pattern both n-Si stripes and graphene, whereas TI35E series positive PR was used as an image-reversal resist in order to achieve an undercut upon development. This undercut layer helps avoiding "bunny ear" effect upon thin metal film deposition and facilitates the lift-off process.

The patterns were designed with Tanner EDA L-edit layout editor program and transferred into the photoresist layer based on a maskless photolithography process using maskless aligner system (Heidelberg μMLA). The details of characteristic dimensions of the device structure are shown in Figure 3.3. For 1D PDA structures, each element has a Si dimensions with length and width of 5 mm and 1 mm, respectively. The length between elements is kept constant as 1.5 mm, but each Si element in the 2D PDA structure has a dimension with length and width of 1 mm. The length between pixels is ~1 mm. In the writing process, the stage hosting the substrate is raster scanned in the x-y plane in ~1 μm precision while the LED source (λ = 365 nm) sequentially exposes the PR pixel by pixel.

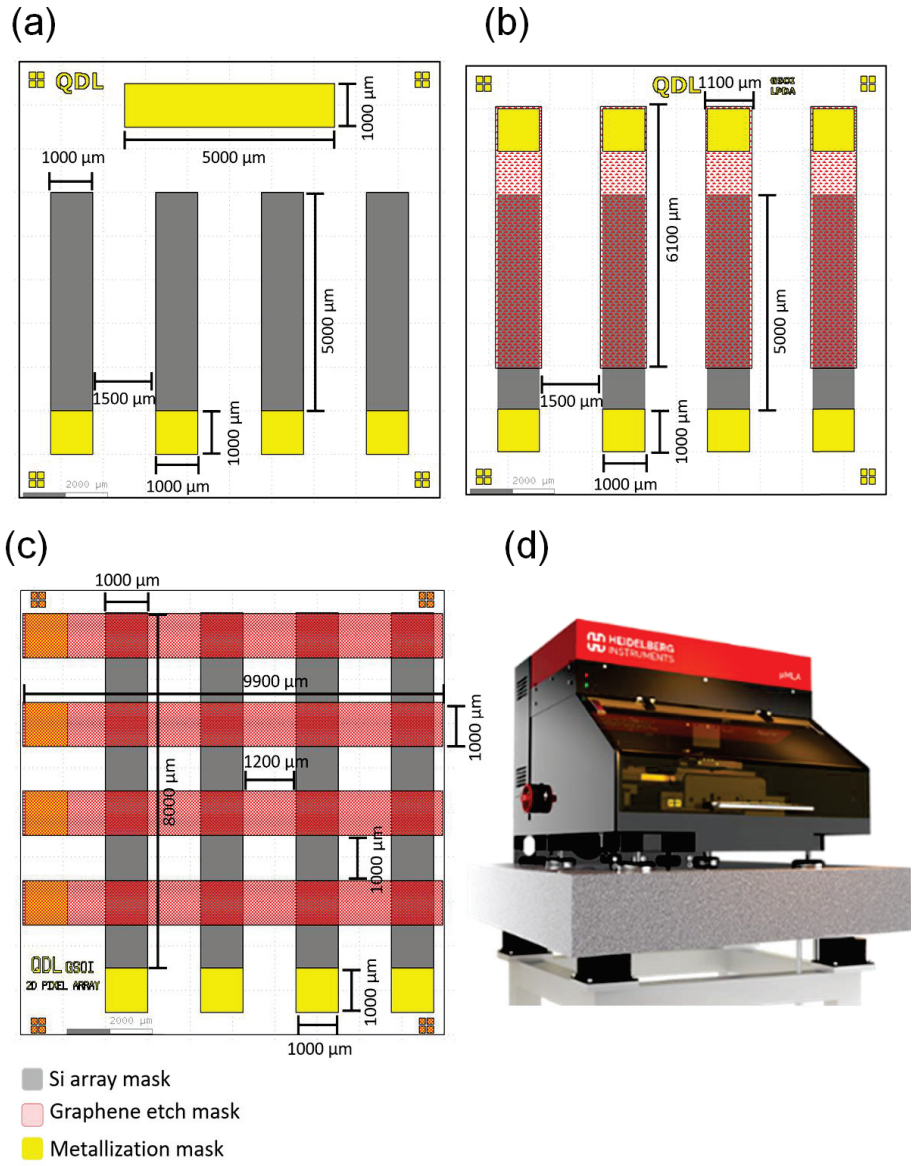


Figure 3.3. The design of the fabricated 1D- G/n-Si PDAs with (a) *common*, (b) *separate* graphene electrode and (c) 2D-pixel PDA device drawn by L edit program (graphene etch mask is dashed as red rectangular shape) and (d) Heidelberg µMLA maskless writer system.

Following the exposure, development of the exposed pattern is performed by immersing the substrate in developer solutions for ~60 s (for thinner PR) or ~20 min (for thicker PR) depending on the thickness of the resist. To stop the chemical reaction of the resist with the developer, the substrate is then rinsed in DI water and dried using a nitrogen gun. The intensity of the focused light beam and the development time are critical factors determining final resolution of the patterns written in the resist. The result of the development was inspected using an optical microscope to determine if further exposure

or development is needed. A general sequence of the photolithography process for each PR type and the subsequent etching steps and metallization are depicted in Figure 3.4.

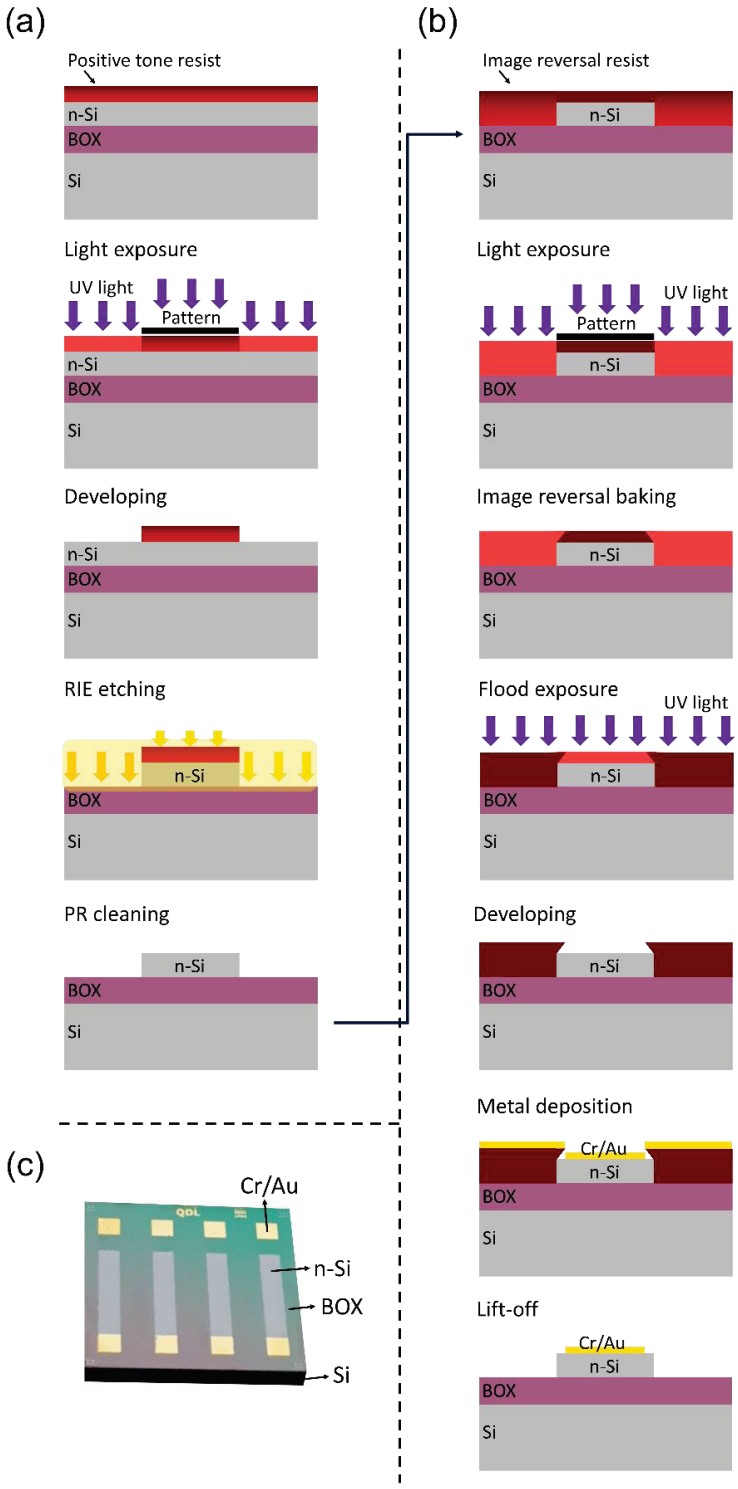
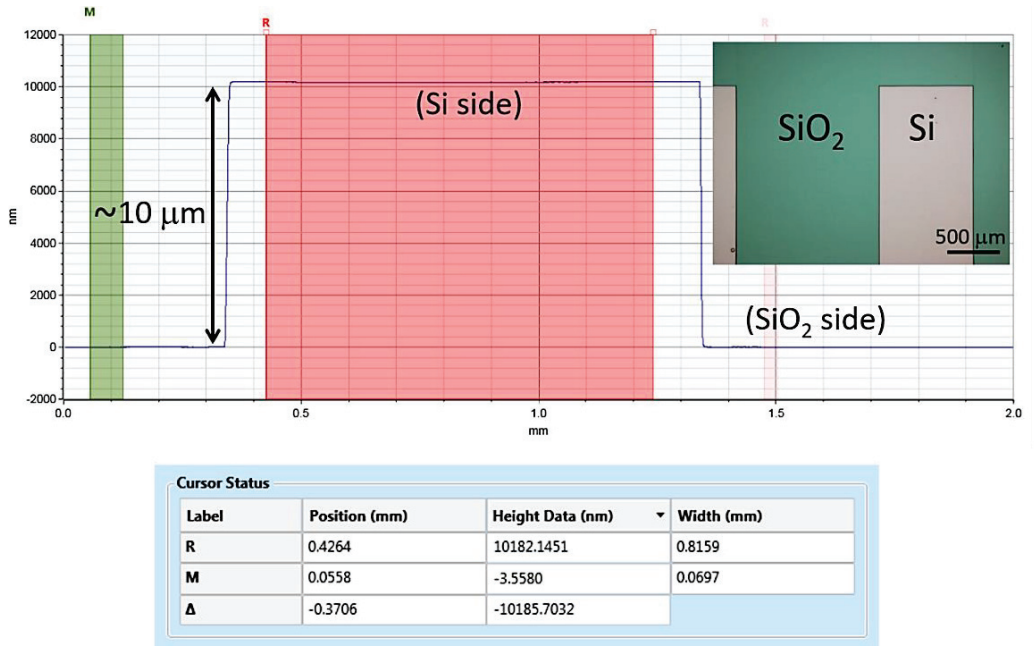


Figure 3.4. Illustration of a typical photolithography process for SOI patterning and metal deposition. (a) Patterning positive tone resist for dry etching of the oxide layer. (b) Photolithography for the metal deposition. Image reversal process is applied to a positive photoresist in order to achieve sufficient undercut structure. Excess metal sitting on the resist is lifted off by removing the resist in acetone bath (c) a photograph of a typical device prepared on SOI substrate.

The details of the fabrication step for 1D and 2D PDA devices are given in the following sections 4.2, 4.3 and 4.4 of chapter 4.

3.1.3. Si array patterning

As mentioned in section 3.1.2, we shaped our samples with PR acted as mask for dry etching. Here, an array of n-Si channels on SOI substrates was obtained by etching Si layer till to reach the BOX layer using Reactive Ion Etching (RIE) (Sentech Ins.) system. The RIE system produces anisotropic etching with vertical sidewalls which is advantageous for hard mask preparation. Etching in this process is based on creation of a plasma with ionized ions of reactant molecules. The etching mechanism is a combination of chemical (reactive) and physical (bombardment) processes [103]. In this context, to reach a thickness of 10 µm thick n-Si substrate patterned side was protected with thick PR and etched directly (~10 µm) to reach the BOX layer (see Figure 3.5). The parameters that were applied for the preparation of arrayed structures are given in the following manner: 10 µm etch was performed under 15 sccm O_2 flow, 50 sccm SF_6 flow with 10^{-8} mbar chamber pressure and 100W RF power during 20 min and 10 min, respectively. After etching procedure, the final thicknesses of the samples were measured by using a DektakXT Surface Profilometer (Bruker).



Cursor Status

Label	Position (mm)	Height Data (nm)	Width (mm)
R	0.4264	10182.1451	0.8159
M	0.0558	-3.5580	0.0697
Δ	-0.3706	-10185.7032	

Figure 3.5. Surface profilometer result of n-Si arrayed SOI structure (inset shows the optical microscope images with 5x magnification).

3.1.4. Growth of graphene by CVD Method

Chemical vapor deposition (CVD) is the most widely used technique for synthesizing graphene sheets, owing to its numerous advantages such as high purity, high uniformity, low defect density, and low cost. As mentioned in detail in section 2.2.4, CVD involves the decomposition of hydrocarbon gases on a substrate at high temperatures, which leads to the formation of a graphene layer. The resulting graphene sheets are highly uniform and have low density of defects, making them suitable for various applications [61]. Here, we used Lindberg/Blue TF55035C Split Mini Tube CVD system for the graphene growth process as shown in Figure 3.6.

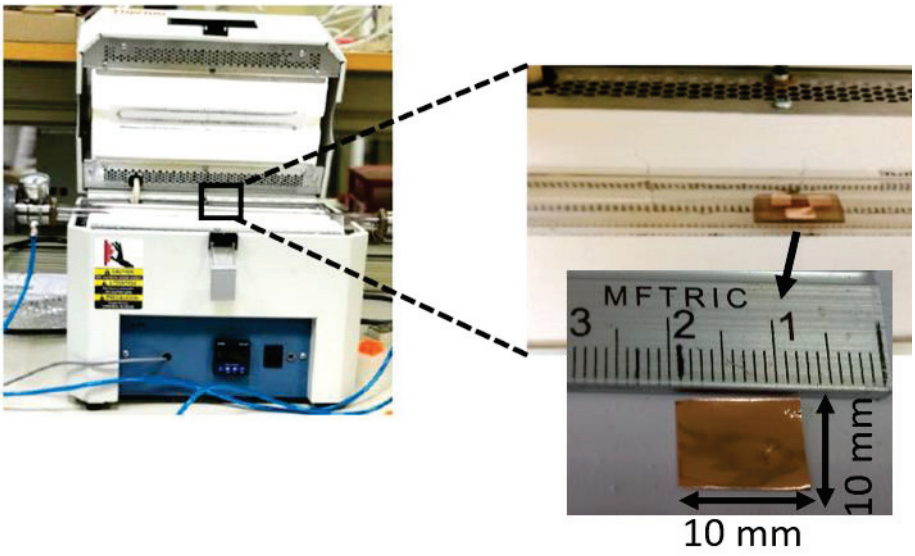


Figure 3.6. The experimental setup for CVD graphene growth in our laboratory contains a furnace with quartz tube, thermocouple and mass flow meter (MKS Instruments). The Cu foils placed on a quartz slide are inserted into quartz tube.

The representative graph on graphene growth process via CVD involving heating, annealing, growth and cooling in the four steps was depicted in Figure 3.7 (a). For our studies, self-limiting growth of monolayer graphene with a surface coverage of higher than 95% was grown on a high purity, 25 μm thick unpolished Cu foil (99.8 purity, Alfa Aesar) by Atmospheric Pressure Chemical Vapor Deposition (APCVD) method (Figure 3.7 (b)). As for the first step, the Cu foil was heated up to 1000 ^{o}C under a flow of H_2 (20 sccm) + Ar (1000 sccm) gas mixture with a temperature ramp rate of 30 ^{o}C min^{-1}. Then the foil was annealed under the same temperature and flow rates for one hour. This

provides both removing of the native oxide layer on the Cu foil and forming of (111) oriented grain boundaries (see Figure 3.7 (c)). After the annealing process, CH_4 (10 sccm) was introduced into the tube furnace for two minutes in order to facilitate the graphene growth. Finally, the sample was left for rapid cooling from growth temperature to R.T. under gas flows of H_2 (20 sccm) and Ar (1000 sccm). In our study, large area monolayer graphene was grown on up to 1 cm^2 sized Cu foil. After the temperature of the furnace reached nearly 100 ºC, the sample was taken from the furnace and then Microposit S1318 PR as supporting layer was drop casted on the G/Cu stack. Then the stack was annealed at 70 °C overnight in an oven to be ready for transfer procedure.

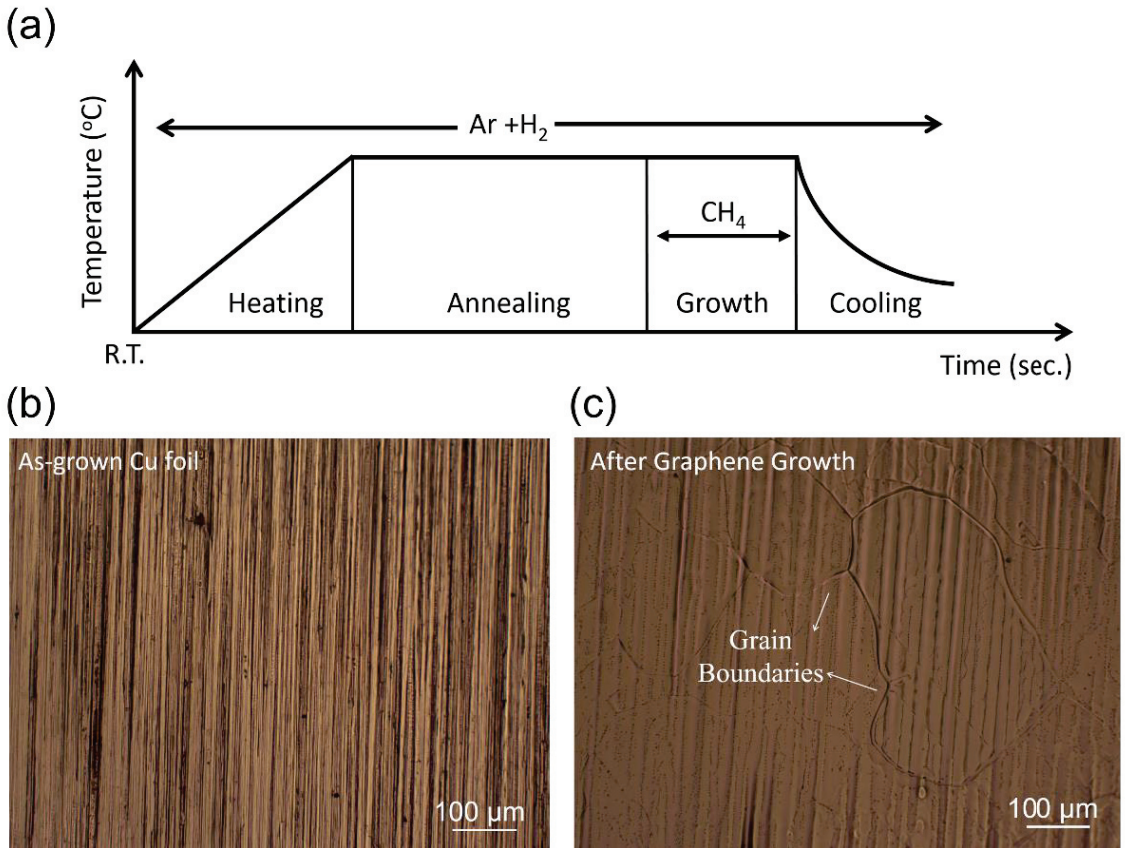


Figure 3.7. Temperature–time diagram of the graphene growth and optical microscope images of Cu foil before and after growth stages.

3.1.5. Deposition of metal contacts

In this study, PDs consist of G and Si contacts. To define metal contacts for each terminal, distinct photolithography steps are carried out, followed by n-Si patterning, metal deposition and lift-off. Figure 3.8 shows the thermal evaporation system that was

used to deposit the metal contacts in QDL. The evaporation chamber contains (1) substrates placed in the sample holder are held inverted at the top of the vacuum chamber, (2) tungsten wire basket for evaporation of SiO, (3) chromium plated tungsten rod and (4) tungsten boat for evaporation of Au. A thermal evaporator utilizes tungsten boats to hold metals heated through a resistive heater to evaporate. The current intensity can be altered to control the evaporation rate. In this systems, the evaporation process occurs in a vacuum environment, and the sample is placed upside down above the target metal crucible. The evaporated atoms condense on the substrate surface to form a thin film, while the deposition rate is monitored inside the chamber using a quartz crystal microbalance (QCM) sensors.

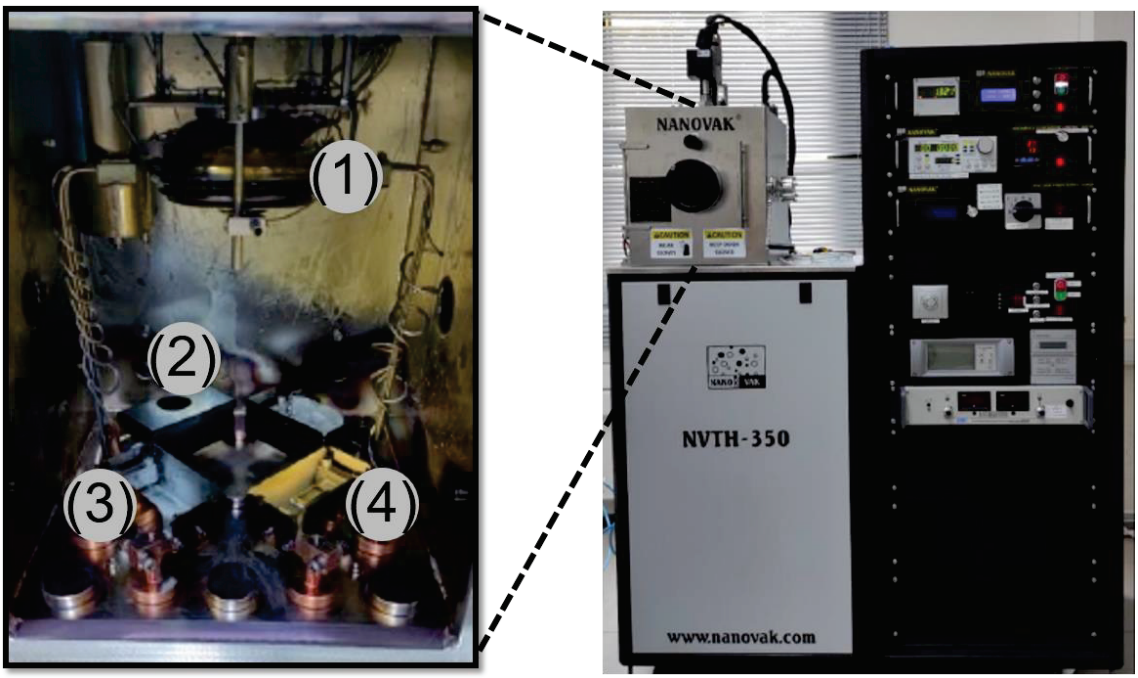


Figure 3.8. The NVTH-350 thermal evaporation system in QDL.

Our fabrication route allows especially in the case of the G/n-Si devices an initially homogeneous natural oxide layer of well-defined thickness of ~2 nm [104]. This oxide layer can reduce the metal deposition quality and tailors the electrical properties between n-Si and metal contact layers. Therefore, to ensure good electrical contact on the n-Si substrate, the native oxide on the device layer is removed using a 6% diluted hydrofluoric acid (HF) solution. Following this, the substrates are promptly loaded into the thermal evaporation system for depositing Cr/Au metallic contact pads. This process is crucial in preparing the substrate for graphene transfer and ensuring the efficacy of the resulting electrical contact. In our study, a thermal evaporator was used to deposit

Cr (4 nm)/Au (80 nm) metals both on n-Si channel and BOX (SiO_2) sides of the SOI substrates. A lift-off process is implemented to create 1D and 2D PDA device structures. Here, 4 nm thick of Cr was used to enhance the adhesion of Au to the substrate prior to the vaporization of Au. Cr was preferred as an initial contact layer due to its good adhesion to both Si and SiO_2. For the remaining contact, Au was chosen because it is an inert metal that is not prone to oxidation under ambient conditions. The goal was to create a Schottky junction by positioning one end of the graphene onto the n-Si surface without touching the metal electrodes deposited on the n-Si, while the other end was in contact with a Cr/Au pad on the BOX layer, which serves to insulate direct contact between the metal electrode and the n-Si substrate.

3.1.6. Wet transfer of CVD graphene

In order to fabricate graphene/n-Si based 1D and 2D PDA on SOI, graphene should be transferred on the SOI substrate. PR is the mostly utilized as a supporting layer during the graphene transfer process and is applied with drop or spin coating on the G on Cu substrate. In our study, graphene was transferred onto desired substrates by using PR 'drop casting' method as shown in Figure 3.9. After graphene growth, thick droplets of Microposit S1813 PR were drop-casted on graphene holding Cu surfaces overnight in the oven at 70 °C to gently harden the PR. Then hardened PR on graphene holding Cu was put into the $FeCl_3$ solution for etching of Cu foil. When the Cu foil was completely etched away, graphene holding PR was put into DI water for 30 min. to remove the $FeCl_3$ or possible Cu residues and etchant contaminations. After rinsed in DI water and then a mixture of H_2O: HCl (3:1) for the removal of $FeCl_3$ residues, the PR/G became ready for transferring onto the arrayed surface of n-Si substrate. Following the deposition of Cr/Au pad on SiO_2 and n-Si layer, the PR/G is annealed at a temperature of 100 °C for 5 min. in order to provide better adhesion of the graphene layer on the surface of n-Si substrate. After the transfer of graphene electrode, the supporting photoresist layer was removed by acetone, followed by rinsing with IPA and DI water and drying it with nitrogen. Then, transferred sample is then left to self-drying for 30 min. to allow evaporation of the trapped water at the interface of the G and substrate, which leads to better conformation of the supporting polymer to the substrate and attending of the wrinkles.

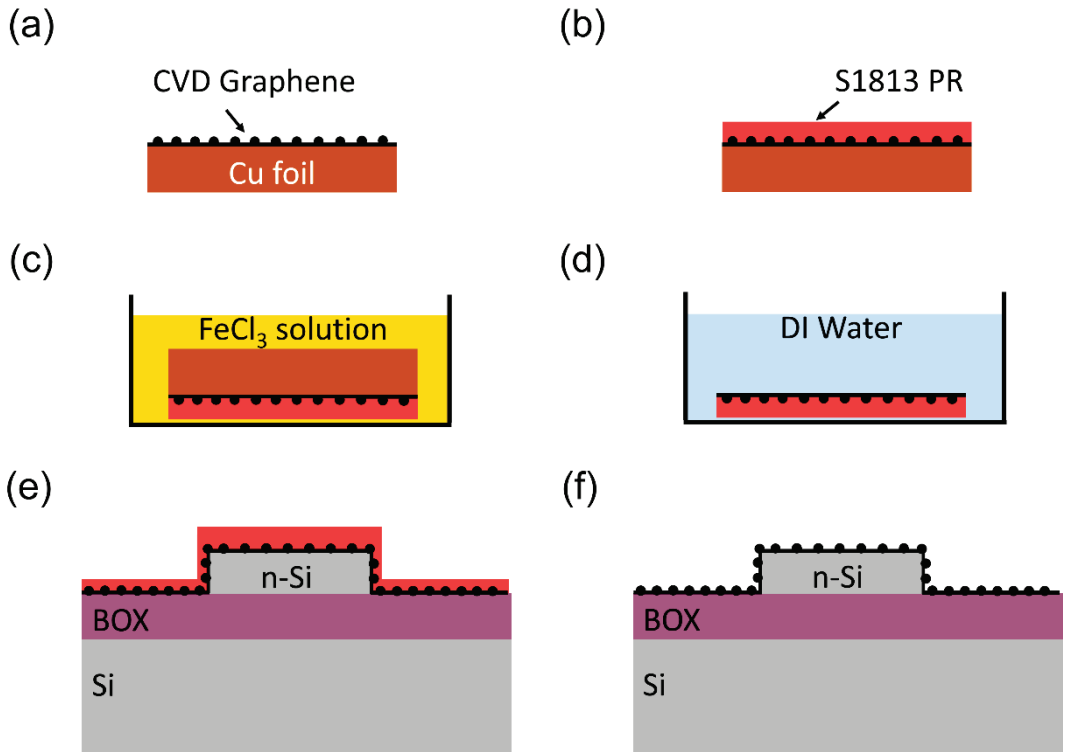


Figure 3.9. Schematic illustration of the graphene transfer procedure. (a) Firstly, CVD grown graphene is placed on a Cu foil. (b) Next, S1813 PR is drop-casted on one side of the foil. (c) After that, the Cu foil is etched, leaving the PR/G stack floating in solution. (d) The PR/G stack is then rinsed in a DI water bath after the Cu foil is completely etched. (e) Subsequently, the PR/G stack is transferred onto the target substrate and left to self-dry. (f) Finally, the PR layer is removed using acetone treatment after baking the sample to improve graphene adhesion onto the substrate surface.

3.2. Surface characterization

After the transfer of graphene onto the patterned SOI substrate, it is crucial to ensure that the graphene film is present and of high quality. In order to prevent contamination, holes, and cracks to produce high-performance devices. Because of the fact that optical microscopy, scanning electron microscopy (SEM), and Raman spectroscopy measurements were conducted in our work to verify the presence, continuity, and quality of the graphene film after the device fabrication procedure.

3.2.1. Optical microscopy

Optical microscopy is a useful tool for characterizing the graphene layer due to the contrast difference between graphene and the substrate. It is a straightforward, rapid, and non-destructive technique that allows for the acquisition of surface images of the graphene layer. Even a monolayer of graphene placed onto an n-Si substrate produces a distinguishable contrast with respect to the color of the substrate. Therefore, optical microscopy is an important technique for quickly and easily assessing the presence and quality of graphene on the substrate surface. Any defects in transferred graphene layer can directly impact the performance of the fabricated G/n-Si PDAs, as discussed in chapter 4. Therefore, ensuring the quality and homogeneity of the graphene layer is crucial for achieving highest device performance.

In our work, an Optika B-500 Optical Microscope was used to quickly observe the graphene and determine any disruptions in the structure, such as defects, residues, and holes. The homogeneity of the transferred graphene onto the Si substrate was also determined by observing whether the contrast of graphene is consistent across all regions. As a result, it is possible to investigate the presence and quality of the transferred graphene on the entire device surface using optical microscope (Figure 3.10).

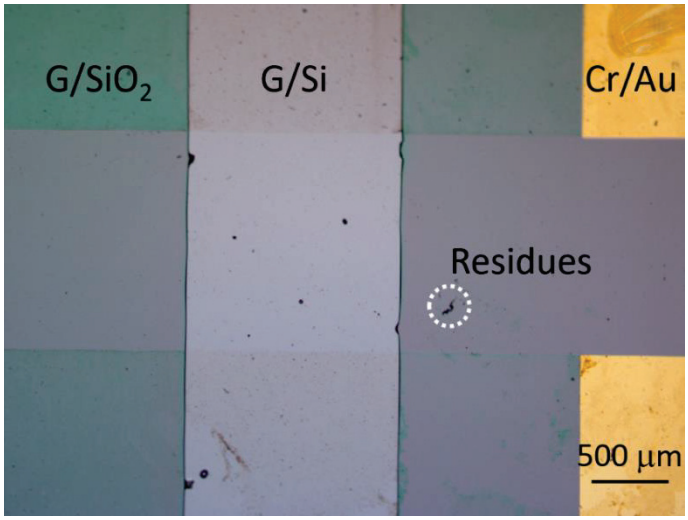


Figure 3.10. Optical microscope image of patterned graphene on SOI substrate (sample: 2D PDA).

3.2.2. Raman spectroscopy

Raman spectroscopy is a non-destructive technique that uses a laser beam to interact with the molecules in a sample. The scattered light that results from this interaction is then analyzed to determine information about the molecular vibrations in the sample. This technique is widely used to study the structure and composition of materials, such as graphene and other 2D materials, as it provides valuable insights into the atomic and electronic properties of the sample without damaging it. The majority of the light that scatters is at the same energy level as the incident photon, and this phenomenon is called Rayleigh scattering. Raman scattering occurs when a small amount of light is scattered at energies different from that of the incident photon. The amount of energy shift in the scattered light is dependent on the vibrational, rotational, or electronic energy of the molecules that caused the scattering. When plotted the intensity of shifted light versus the wavenumber, a Raman spectrum of the material can be obtained.

Raman spectroscopy is widely used to characterize graphene, giving the information about number of graphene layers, continuity and quality of graphene. The Raman spectrum of graphene typically exhibits three main peaks at specific wavenumbers namely D peak (~1350 cm^{-1}), G peak (~1590 cm^{-1}) and 2D peak (~2700 cm^{-1}) [105]. The D peak is known as defect related peak or a structural disorder in graphene. It is typically very weak in high quality graphene. G peak indicates in-plane vibrations of sp^2 bonded C-C atoms in graphene lattice and 2D peak is the second order of D peak, which gives information about number of graphene layers. A strong G peak and weak D peak in the Raman spectrum of graphene and the single Lorentzian 2D peak with a full width at half maximum (FWHM) of ~29 cm^{-1} confirm high the quality of monolayer graphene [106].

In our work, Raman measurements of the samples were performed using a Renishaw (New Mills, UK) inVia confocal micro-Raman spectroscopy to determine the number of G layers, homogeneity and quality of graphene on each array and pixel in the point scan and mapping mode. Single-point Raman spectroscopy measurement was performed to determine the number of graphene layers, homogeneity and quality of CVD graphene on a typical GSi Schottky junction device where graphene covers both Si and SiO_2 regions. Raman signals were recorded using an Ar^+ ion laser with a 532 nm excitation wavelength laser source. Raman measurements were repeated several times at different locations on the array to ensure continuity. In all the measurements, graphene-related D, G, and 2D peaks were found at the peak wavelength of around ~1365, ~1596

and ~2715 cm^{-1}, respectively as shown in Figure 3.11. The analysis of the 2D peak can be seen as the inset of Figure 3.11. Here, the 2D peak can be fitted with a single Lorentzian function. The FWHM value and the R^2 coefficients correspond to the quality of the fitted experimental data. The large 2D to G peak intensity ratio ($I_{2D}/I_G > 2$) confirms the single-layer thickness of the graphene layer [107].

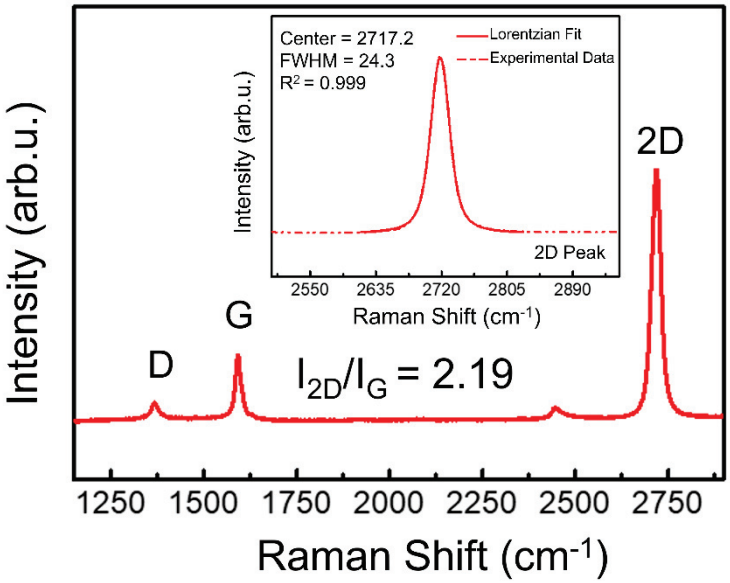


Figure 3.11. A typical single-point Raman spectrum of transferred graphene on arrayed SOI substrate.

3.2.3. Scanning electron microscopy

The structural analysis of G/n-Si pixels and n-Si element were done with scanning electron microscopy (SEM) measurements (Nova NanoSEM 650, FEI). The surface quality of the G/n-Si pixel can be effected by the chemicals used in transfer and patterning procedures applied in the fabrication route. According to the Raman spectroscopy results, it was found that graphene layer was free of defects after transferring on SOI. However, there could be some local defects, cracks or residues which decreases the photo response of the pixels in the array. Graphene related wrinkles can also be seen in the high magnification SEM image (Figure 3.12). These observed wrinkles are clear indicators for the coverage of a graphene layer on n-Si substrate.

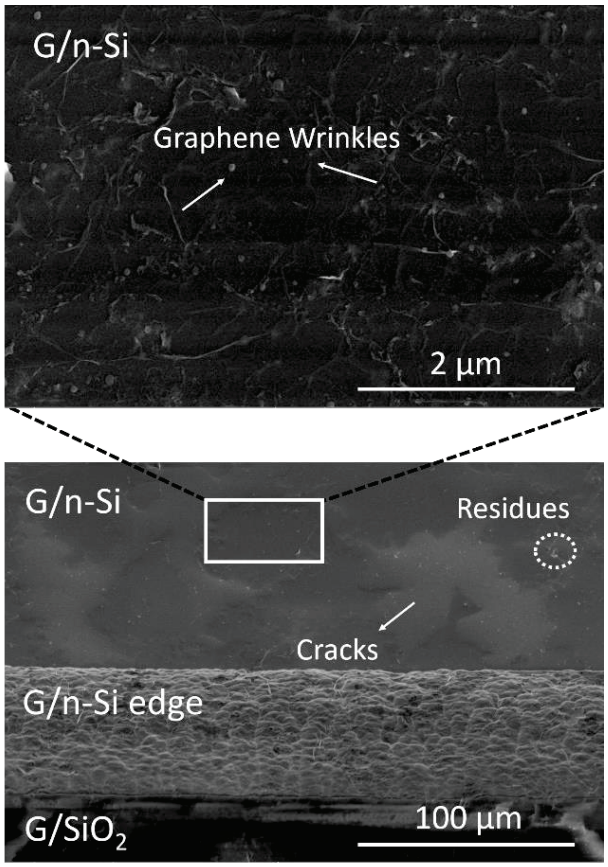


Figure 3.12. High resolution SEM images of G/n-Si diode.

3.3. Device characterization

3.3.1. Current-voltage and spectral response measurements

For two-terminal I–V measurements, 80 µm thick Cu wires were bonded both on the Cu plated paths of a PCB card and Cr/Au contact pads on the sample by means of a lab-built wire bonder. The electronic and optoelectronic characterizations of each G/n-Si diode were performed by tungsten-halogen lamp (Osram, 275 W) at R.T. under ambient conditions and using a probe station interfaced with a wavelength tunable monochromator light source (Newport, Oriel Cornerstone) including internal shutter, Keithley 2400 Source-Meter, Keithley 6485 Picoammeter and Keithley 2182 Nanovoltmeter as depicted in Figure 3.13.

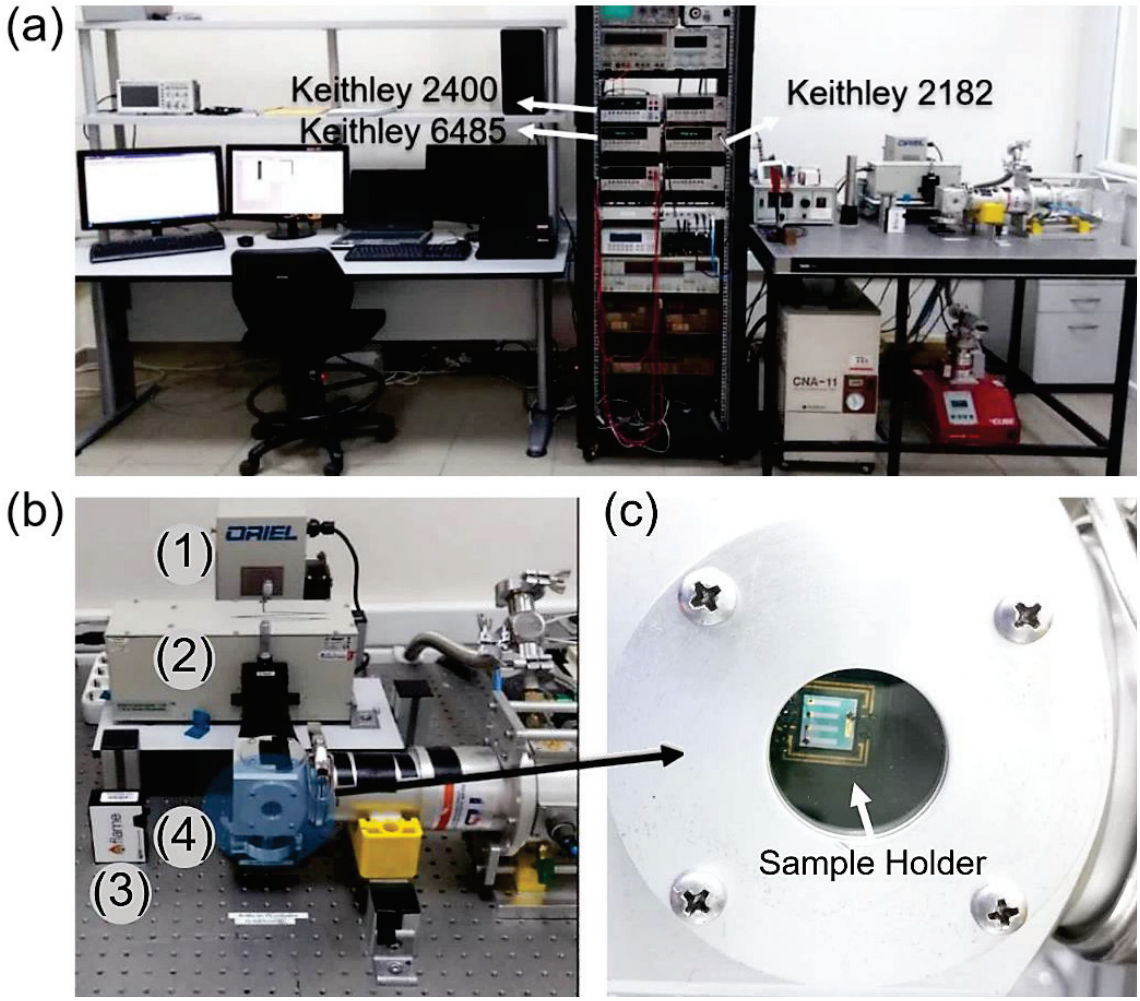


Figure 3.13. (a) Electrical and optoelectronic characterization units in QDL at IZTECH. (b) The setup including, (1) a quartz tungsten halogen lamp (Osram, 275 W), (2) a high resolution monochromator (Newport, Oriel Cornerstone), (3) spectrometer (Oceans Optics), (4) a closed loop sample stage. (c) The image shows the G/n-Si Schottky PDA with *common* graphene electrode after loaded onto sample holder of the system.

The I-V measurements obtained in the dark is used to determine important diode parameters such as rectification, η, SBH and series resistance. In our work, the I-V measurements of the devices were carried out at R.T. under ambient condition. The voltage was applied for all the devices from 0 to 1 V for forward biasing and 0 to - 1 V for reverse biasing. To maintain a dark environment, the device is connected to a closed loop sample holder as seen in Figure 3.13 (c).

The following procedures were applied to measure the spectral R of devices. Firstly, the FWHM of light in the spectrometer was calibrated by tuning the slit mounted on the monochromator and then a commercial Si-PD (FDS10X10, Thorlabs) was used to

determine the incoming power of light on the device area. Here, Si PD is used as reference detector and gives the power output in unit of watt. Therefore, responsivity vs wavelength data for our fabricated devices were obtained based on this power output. All measurements were taken with a filter, which passes 515 nm and above, also in order to suppress unwanted second order harmonics.

3.3.2. Light power dependent I-V measurements

This experiment aims to understand the photoresponse characteristics of single pixel G/n-Si Schottky PD on SOI substrate by comparison with G/n-Si PD on bulk Si. In this setup, a led which has 940 nm wavelength was used as a light source (see Figure 3.14). The photoresponse measurements of all single-pixel G/n-Si Schottky devices were evaluated for NIR wavelengths ranging employing 940 nm LED (1), 905 nm laser line filter (2) (FL905-10, Thorlabs), high power LED driver with pulse modulation (3) (Thorlabs DC2200) and optical bandpass filters. A specific wavelength of 905 nm was provided with a laser filter. As we know that from our reported studies [95, 108], reference G/n-Si PDs give the maximum peak at the wavelength of 905 nm. For this reason, the photoresponse measurements of were acquired under 905 nm wavelength light and the measurement results can be found in section 4.1.2 of chapter 4.

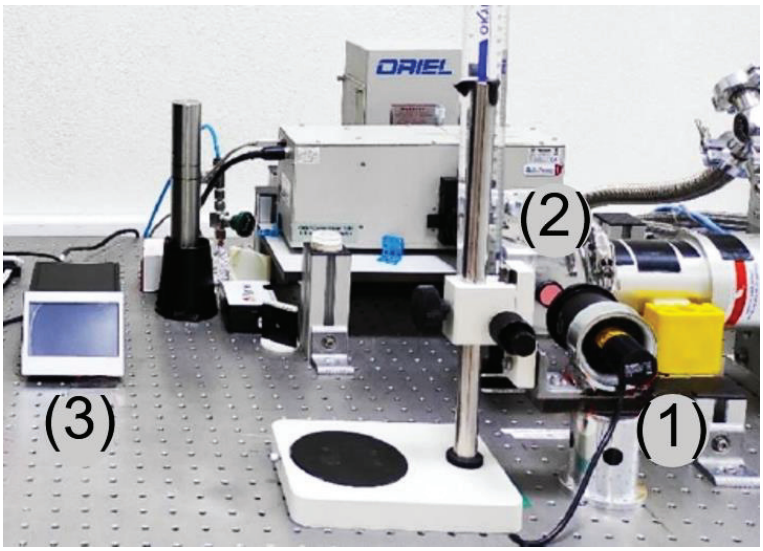


Figure 3.14. The image of the photoresponse measurement setup which contains (1) 940 nm LED, (2) 905 nm laser line filter and (3) high power LED driver with pulse modulation.

3.3.3. Time-resolved photocurrent measurements

Time-resolved photocurrent measurements of the devices were done for deep red wavelengths (λ = 660 nm) 1W Power LED and function generator as LED driver with pulse modulation (Uni-t utg9005c). The photoresponse measurements of devices were acquired under 660 nm wavelength light pulsed with 1 kHz frequency. After the photocurrent obtained as a result of incoming pulsed light on the sample, transimpedance amplifier convert the photocurrent to voltage and amplify the signal, so we read the data from oscilloscope. The measurement setup is shown in Figure 3.15.

The irradiation wavelength is specifically selected to be 660 nm since it corresponds to the maximum R of our fabricated graphene and SOI based 1D and 2D PDA on 10 μm thick substrate. For further information for selecting this specific wavelength can be found in the section of 4.1.3.

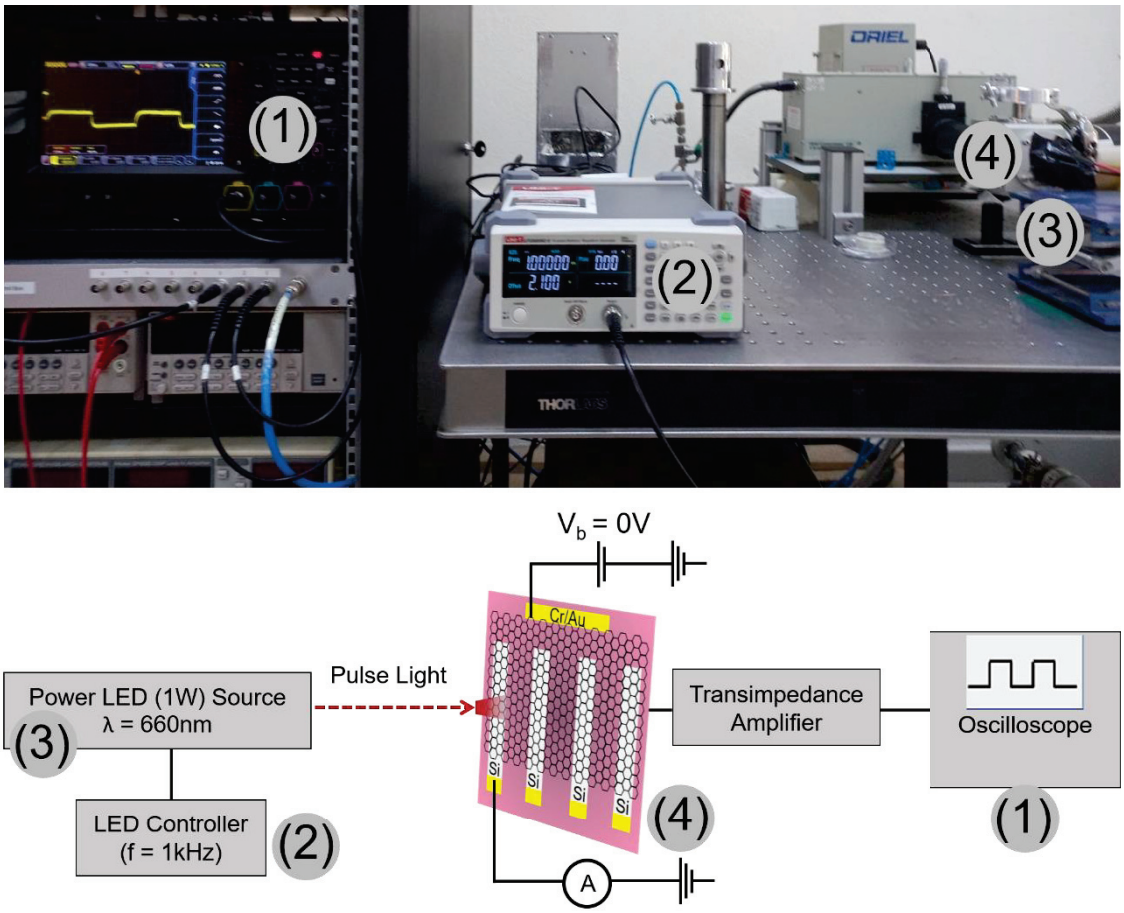


Figure 3.15. The picture and schematic illustration of the time-resolved photocurrent measurement setup contains (1) an oscilloscope, (2) a function generator, (3) a 1W Power LED and (4) our device. (sample: 1D PDA with *common* graphene electrode).

3.3.4. Optical crosstalk measurements

The photoresponse of each individual G/n-Si diodes in the PDA was characterized separately under illumination of light with 660 nm wavelength. For the experiments a LED source was coupled to a fiber optic cable with 600 μm core diameter to maintain local illumination on each G/n-Si diode and on SiO_2 regions between them as depicted in Figure 3.16. To avoid possible optical crosstalk between neighboring n-Si elements, the distance between the sample and the tip of the fiber optic cable was kept at ~1 mm to ensure a well-defined spot size and to minimize possible back reflections that may respectively arise from the illuminated Si surface and the metallic tip of the fiber optic probe used in the experiments.

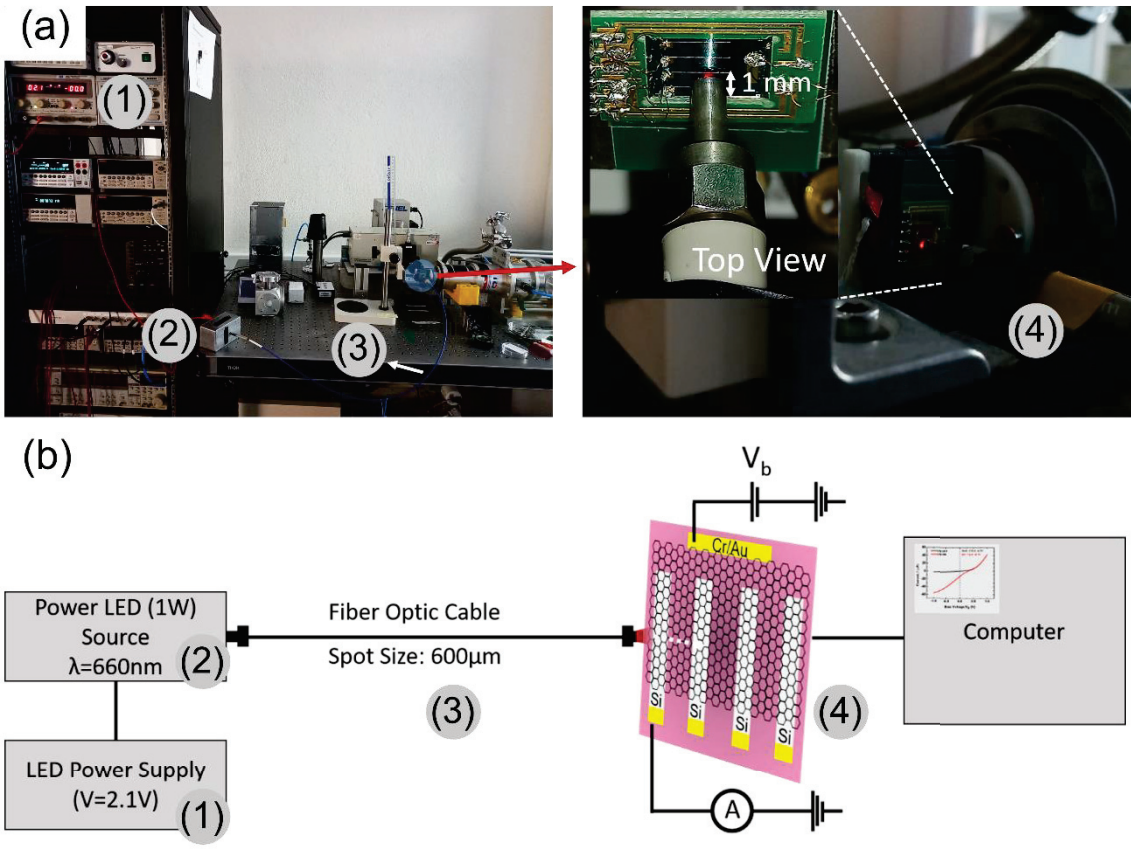


Figure 3.16. (a) Optical crosstalk measurement setup and (b) schematic diagram contains (1) a LED power supply, (2) a 1W LED source, (3) a fiber optic cable with 600 μm core diameter and (4) our device. (Sample: 1D PDA with *common* graphene electrode).

CHAPTER 4

RESULTS AND DISCUSSION

4.1. Single pixel G/n-Si PD on SOI and bulk Si

G/n-Si Schottky PDs have been demonstrated as an efficient architecture for photodetection so far. The typical approach for G/n-Si Schottky device fabrication involves the partially wet-etching of the SiO_2 layer from the Si surface. Following this, G is transferred on the Si surface to create the G/n-Si Schottky junction. However, these devices partially fail to provide sufficient passivation due to the use of thin SiO_2, resulting in electrical leakage in most devices after the metallization process. In order to obtain graphene contact in the device structure, the electrical leakage should be hindered on the SiO_2 side before transferring of graphene. Therefore, most substrates with Si/SiO_2 structure can not be utilized prior to graphene transfer. A solution to eliminate the electrical leakage problem is a replacing commonly employed bulk Si with a SOI substrate. Besides, SOI structure has many advantages as we explained in the section 2.1.

Before the fabrication of PDAs, it is essential to observe the optoelectronic characteristics such as R, D^* and NEP of single pixel G/n-Si Schottky PD fabricated on SOI (GSOI). In this section 4.1, the device performance of GSOI was systematically studied and compared with a reference G/n-Si Schottky PD fabricated on bulk Si (GSi) to understand the photoresponse mechanism. In this regard, the observed results guide section 4.2, section 4.3 and section 4.4, respectively.

4.1.1. Device fabrication

Bare n-doped photo-active silicon (Si (100)) wafers (specification $\rho = 1–5\ \Omega$ cm, extracted doping level $N_d \approx 2 \times 10^{15} cm^{-3}$) have been used for both SOI and bulk Si substrates in order to see the effect of the photoactive layer thickness on device performances. Before cleaning the SOI and bulk Si substrates, a HF dip was used to remove the native oxide on device layer. All samples were cleaned with acetone and propanol to remove eventually present polymer residues from e.g. wafer carriers. The

substrate preparations of GSOI and GSi are depicted in Figure 4.1 (a) and (b), respectively. After, one side was protected with thick PR and etched directly (~10 μm) to reach the oxide layer by RIE system. Concurrently, GSi sample was prepared in the following manner. By means of a thermal evaporator, about 400 nm thick SiO_2 dielectric layer was deposited through a metallic shadow mask to partially cover the surface of an n-Si substrate. For the I–V measurements, Cr (4 nm)/Au (80 nm) metal contact pads were evaporated both on the n-Si side and on the SiO_2 covered the side of both GSOI and GSi substrates. The single graphene layer was transferred onto the prepared substrates using PR drop casting method (see section 3.1.6 for the details) to achieve the device structure. The active area of the junction was measured as ~20 mm^2 after the transfer for both devices.

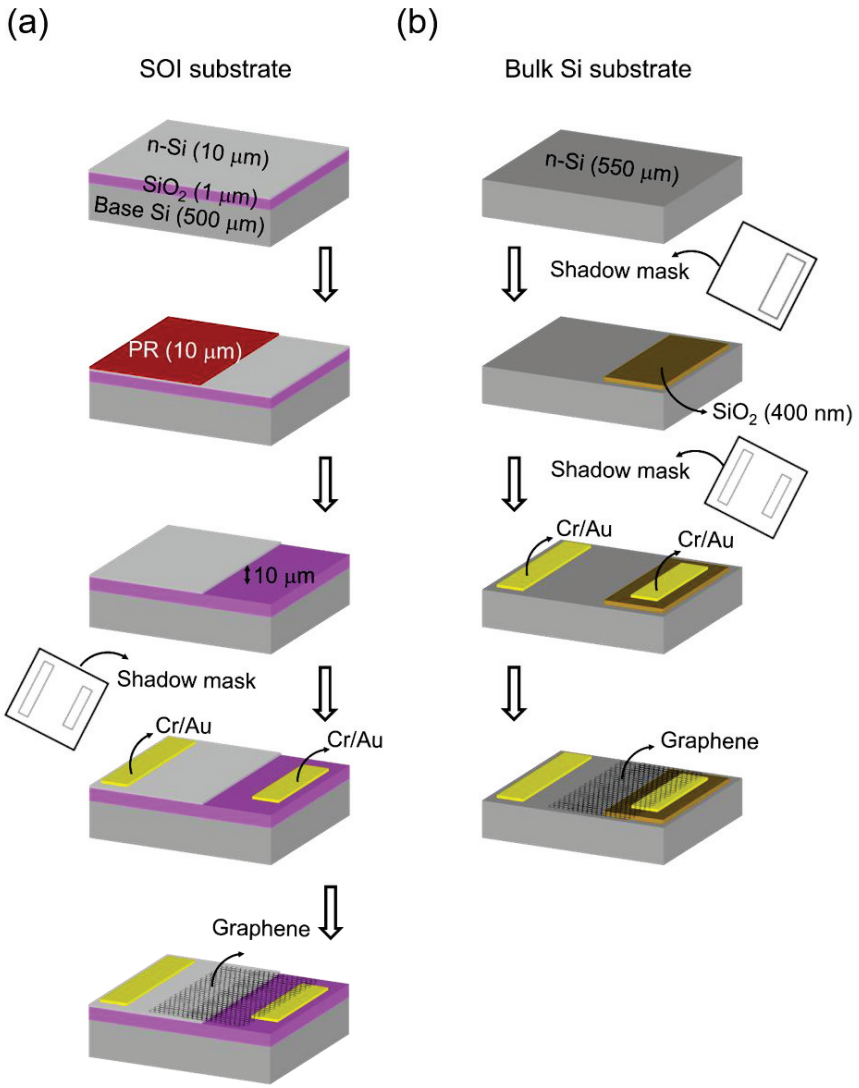


Figure 4.1. The schematics of the fabricated single pixel G/n-Si Schottky PDs; (a) GSOI and (b) GSi, respectively.

The fabricated GSOI and GSi devices with an active area of 20 mm^2 (see Figure 4.2 (a) and Figure 4.3 (a)) and their cross-sectional representations with electrical contacts can be seen in Figure 4.2 (b) and Figure 4.3 (b), respectively. The current-voltage (I-V) measurements of both the GSOI and GSi devices were performed under dark and ambient conditions at R.T. Applied bias voltage was in the range between – 0.5 V and 0.5 V. Both of the I–V curves exhibit the strong rectifying character of a typical Schottky barrier diode but with slightly different current levels varying in the forward bias range (Figure 4.2 (c) and Figure 4.3 (c)). For a detailed comparison, the obtained I–V data were plotted in the semi-logarithmic scale (see the inset of Figure 4.2 (c) and Figure 4.3 (c)). From the I-V plot of the GSOI and GSi PDs, I_d values were determined as 0.9 nA and 0.6 nA, respectively. It is notable from the log(I) vs V plot that the GSOI PD device exhibits a reduced forward and an increased dark current density under reverse bias compared to GSi. The exact reason is suspected that both the inhomogeneous stress, strain and doping profile of graphene due to the thin Si surface in contact with graphene may play a role. Although the current increases linearly at very small bias voltages, in accordance with the well-established TE model. The deviation from linearity observed at high voltages is due to the series resistance contributions from the underlying n-Si substrate.

For an ideal diode η is equal to 1 but it generally has greater values. According to the literature the η values for graphene Schottky junctions are in the range of 1.3− 30 which are far from ideal value [109-111]. Some recent studies have shown that the inhomogeneity at the G/Sc junction [7] is a cause of nonideality. This can lead to high leakage currents and low values for η [91, 111]. High values of η can be explained by the existence of the interfacial thin layer, inhomogeneities of Φ_B distribution and the bias voltage dependence of Φ_B [112]. The *Rs* of the device can be defined as the combination of contact resistance between graphene and Si, resistivity of graphene and Si and resistance of connecting wires [113].

We intentionally employed a fit of equation 4.1 over the linear region of forward bias voltage range despite deviations of the experimental data from ideal diode characteristics and determined *Rs*, η and zero-bias Φ_B of the devices from the dark I-V plots according to TE model [68] given as,

$$I = AA^{*}T^{2} \exp\left(-\frac{q\Phi_B}{kT}\right)\left[exp\left(\frac{qV}{\eta kT}\right) - 1\right] \qquad 4.1$$

A is the active junction area (0.2 cm^2 for our G/n-Si PDs), A^* is the effective Richardson constant (112 A/cm^2K^2 for n-Si), T is the temperature (300 K), Φ_B is the SBH at the junction between G and n-Si, k is the Boltzmann constant, q is the elementary charge and η is the ideality factor. The Schottky diode parameters η and Φ_B for the fabricated G/n-Si PDs were extracted using the method developed by Cheung [89] in the case of non-negligible R_s. The Cheung's function is given as,

$$\frac{dV}{dln(I)} = IR_s + \eta\frac{kT}{q} \tag{4.2}$$

the R_s and η from the slope and the intercept of the straight line fitting *dV/dln(I)* vs *I* plot was determined using equation 4.2, respectively. The values of η and *Rs* for GSOI were obtained as 2.90 and 40 kΩ, respectively. On the other hand, these values for GSi were obtained as 1.45 and 60 kΩ for the GSi device, respectively. The reasons for the high *Rs* of our devices when compared with the literature [12] may be defects in graphene occurred during transfer procedure or adsorbed molecules (H_2O and O_2) on the graphene which give rise to degradation on devices performance, resulting in high *Rs* at the graphene-Si interface. Even if the active area is the same in all devices, the differences in junctions can be formed in GSi junction and effectively lead to an electrical equivalent circuit representing a parallel circuit of Schottky diodes with different *Rs*, η, and Φ_B. These differences can be especially occurred due to the device fabrication process. Further, especially in the GSOI device, inhomogeneous stress and strain caused by the RIE etching of Si substrate may alter the surface topography and cause the possible imperfect contact and interfaces between graphene and the Si substrate which effects the current transport in junction. The Φ_B of the junction is also determined using the *H(I)* function stated in equation 4.3,

$$H(I) = V - \eta\left(\frac{kT}{q}\right) ln\left(\frac{I}{AA^*T^2}\right) = IR_s + \eta\Phi_B \tag{4.3}$$

from the intercept of the linear region of *H(I)* vs *I* plot for GSOI and GSi PDs as shown in Figure 4.2 (d) and Figure 4.3 (d), respectively. Accordingly, the zero-bias Φ_B was calculated as 0.88 eV and 0.81 eV for GSOI and GSi PDs, respectively. The Φ_B of the heterojunction of single-layer CVD grown graphene on n-Si has been reported to be either 0.79 or 0.88 eV under zero-bias and at R.T. for the identical substrate doping level of $N_d \approx 2 \times 10^{15}$ cm^{-3} in the literature [7, 110].

Considering the Schottky–Mott model, where Φ_B is defined as the difference between the Φ_G and the χ of Si (χ_{Si} = 4.05 eV), Φ_G was calculated as 4.93 eV and 4.86 eV for GSOI and GSi PDs, respectively. GSOI and GSi PDs had high sensitivity due to the low dark current of ~0.9 nA and ~0.6 nA, respectively. Such an increment of dark current of GSOI is attributed to the presence of surface states with high density and the thinner active layer in the junction [114].

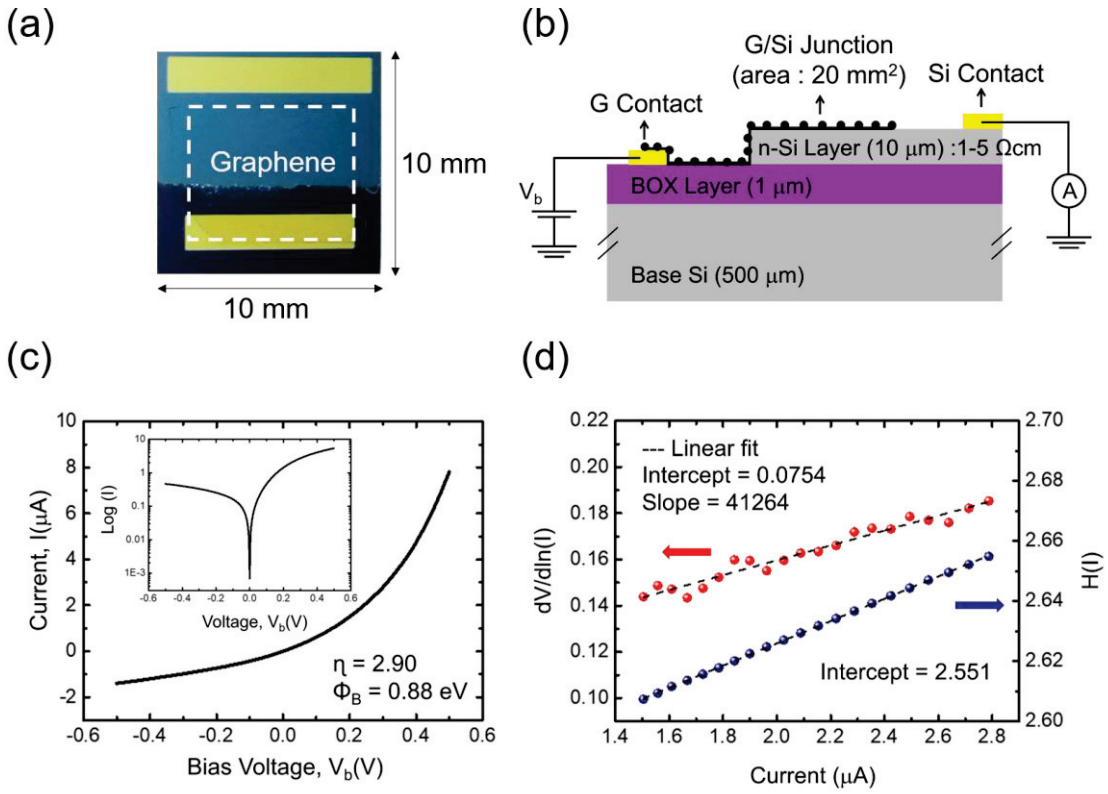


Figure 4.2. (a) Device picture and (b) the cross-sectional image of the fabricated single pixel GSOI Schottky junction PD after electrical connections. (c) The I-V curve of the device in dark. Inset shows the forward bias log(I)-V plot. (d) Plots of *dV/dlnI* and *H(I)* as a function of current which were used to extract diode parameters according to Cheung's method.

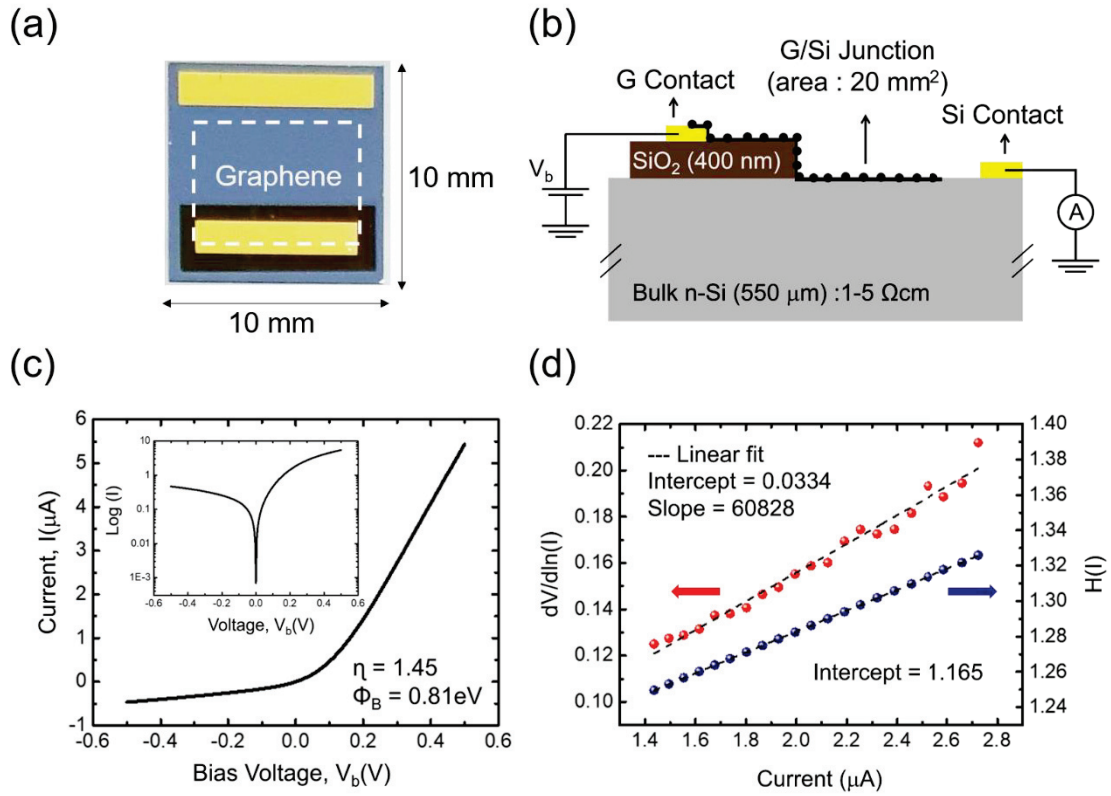


Figure 4.3. (a) Device picture and (b) the cross-sectional image of the fabricated single pixel GSi Schottky junction PD after electrical connections. (c) The I-V curve of the device in dark. Inset shows the forward bias log(I)-V plot. (d) Plots of *dV/dlnI* and *H(I)* as a function of current which were used to extract diode parameters according to Cheung's method.

4.1.2. Photoresponse characteristics of the devices

The measurement setup was given in Figure 3.14 of section 3.3.2. The variation in the I-V characteristics of the GSi and GSOI PDs under illumination with λ =905 nm led light at optical powers varying from P = 0.5 μW–50 μW were displayed in the semi-logarithmic scale in Figure 4.4 (a) and (b), respectively.

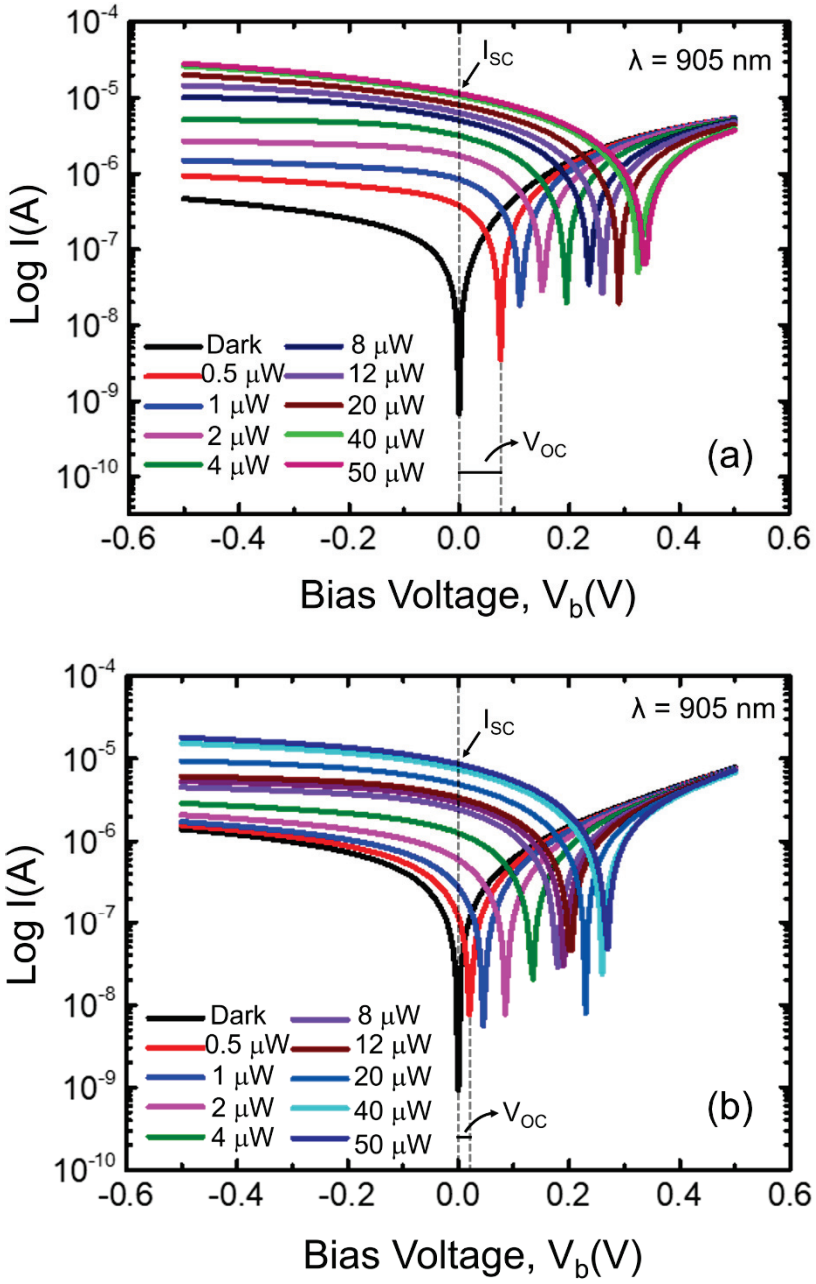


Figure 4.4. I–V characteristics of single pixel (a) GSi and (b) GSOI PDs under different light powers.

Thanks to the optical transparency of the thin graphene layer, incident led light is expected to be absorbed in the n-Si substrate, where it generates the photocurrent observed under bias conditions. GSi device exhibited a clearly distinguishable photoresponse under 905 nm wavelength compared to GSOI one.

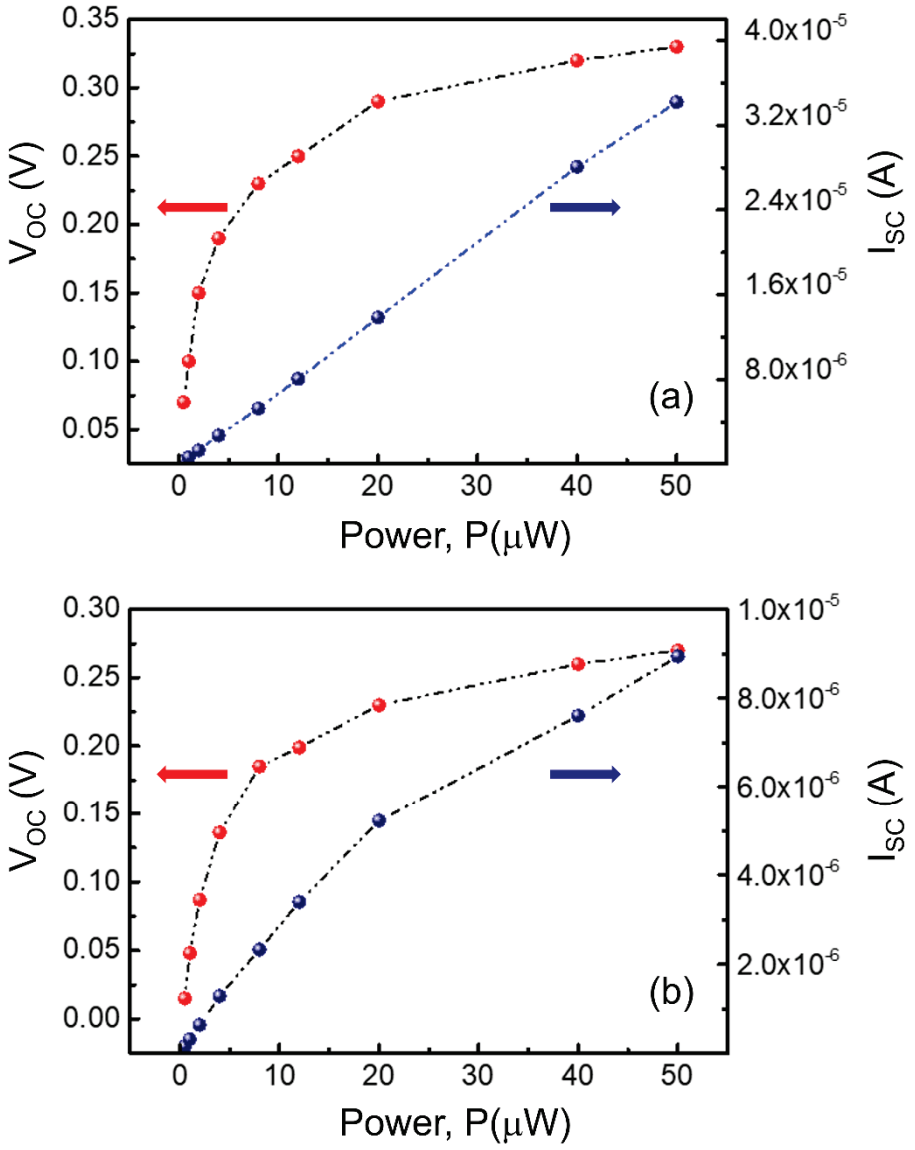


Figure 4.5. I_{SC} and V_{OC} of (a) GSi and (b) GSOI PDs exposed to 905 nm wavelength light with different powers, respectively.

Figure 4.5 (a) and (b) shows the relation of I_{SC} and V_{OC} versus different powers of GSi and GSOI PDs under 905 nm wavelength, respectively. For both devices, V_{OC} increases nonlinearly and converges to a saturation level over ~0.25 V at the light power of 40 μW. Although I_{SC} value of GSi exhibits a clear linear response to the incident light, the linear behavior of I_{SC} value for GSOI varies at the light power of 20 μW. The slope of I_{SC}-P plot can give the idea about the R value of the PD devices. That's why, the linear behavior of I_{SC} vs P plot is a great importance in terms of the reliability and repeatability of the PD devices. The reason for the lowest photoresponse for GSOI PD is also related

with the depth of depletion layer (X_d) occurs at the GSi interface. Briefly, the larger X_d absorbs more photon [70] and that mechanism will be discussed in section 4.1.3.

4.1.3. Responsivities in the Si absorption range (400-1100 nm)

The spectral response of the PDs on SOI substrate in comparison with a device fabricated on 500 μm thick bulk n-type Si with identical doping level is shown in Figure 4.6. Using the equation 2.18 of section 2.6, the spectral R of GSOI and GSi devices were measured at zero-bias (V_b = 0V) as a function of the λ of incident light varied in the spectral range between 400 and 1100 nm. The obtained maximum responsivity (R_{max}) of GSOI PD reaches 0.52 A/W at the wavelength of 660 nm, in correlation with typical optical absorption spectrum of n-type Si, respectively. In another peak appeared at ~780 nm (circled with green color in Figure 4.6 (a)) is related with the photon penetration depth. For GSi device, the obtained R_{max} at the wavelength of 905 nm is about 0.68 A/W (Figure 4.6 (a)). However, the respective *R* exhibits a downward trend below the cutoff wavelength of 1100 nm that corresponds to an energy level which is below the band gap energy of Si. GSOI and GSi PD exhibits typical Si based *R* behavior similar to that reported in literature [12, 95]. The measured responsivities were normalized with the maximum values to obtain the shift in R_{max} value of fabricated devices. As manifested in Figure 4.6 (b), it is further noticeable that the spectral response of GSOI devices shifts towards the visible regime depending on the photoactive Si thickness compared to GSi device.

For GSi, the *R* with linear character is present up to a wavelength of 905 nm and then decay due to the Si absorption edge. Although the active area of the devices was the same, it is clear that the R_{max} of GSOI device is lower than the maximum responsivities of GSi PD. Reducing the photoactive layer Si thickness causes a decrement in the absorption of light [115] and less photogenerated current generated between graphene and Si interface. Accordingly, light-trapping concepts have been introduced that prolong the light path inside the absorber layer [116]. These mechanisms will be discussed in section 4.2.3. Light of longer wavelengths $\lambda > 450$ nm can penetrate deeper into the Si substrate due to the reduced absorption coefficient. For longer wavelengths, only part of the incident light is absorbed within the active top Si layer of the SOI substrate and the remaining light power is transmitted into the BOX and Si handle layer where it does not

contribute to the photoresponse [12]. Hence *R* values of SOI devices begin to decline earlier than GSi fabricated on bulk Si. That is the reason that GSOI device shows the lowest response at the wavelength of 905 nm.

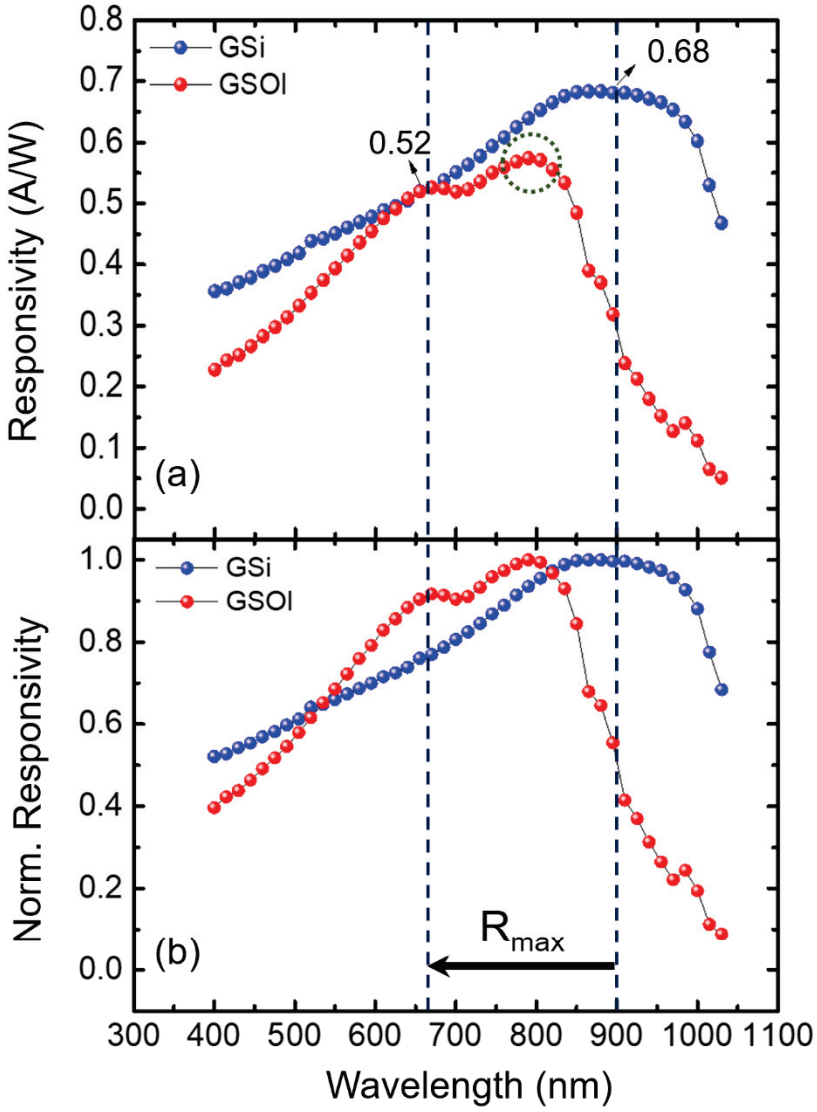


Figure 4.6. Comparison of the device layer thicknesses on the spectral response at zero-bias (V_b = 0 V). (a) Spectral R and (b) normalized R (Active area for both devices is 20 mm^2.)

It is important to note that even though the top Si layer forms an optical microcavity for the GSOI devices that should lead to an oscillating wavelength dependent *R* as mentioned in Ref [12]. This behavior was not observed for GSi device. Selvi et al. theoretically observed that the active Si layer of the GSOI-planar device forms an optical cavity where multiple reflections between the topmost air-Si, Si-BOX and BOX-handle Si interfaces lead to optical interference effects [12]. The behavior of incident and reflected

light in bulk Si and SOI substrate is shown in Figure 4.7. In the case of a bulk Si wafer, when light arrives at the surface of the wafer some of the radiation is reflected at the surface and the remaining part is transmitted through the Si as shown in the schematic, as shown in Figure 4.7 (a). Since the thickness of the wafer is ~500 μm which can be considered to be optically thick, where all transmitted radiation is absorbed in a few tens of microns, there is no reflection from the back surface of the substrate. Therefore, the reflectivity depends only on the optical properties of bulk Si. In the case of a multilayer SOI (Si-SiO_2-Si) structure, the radiation is partially reflected from the surface of Si while the remaining part transmits into the Si layer to face another reflection at the Si-SiO_2 interface. Hence, transmission into the SiO_2 layer to be partially reflected at the next SiO_2-Si interface and the remaining part absorbed into the thick substrate. So each radiation is subject to partial reflection and transmission at each interface Figure 4.7 (b). Tracing all the reflections of each ray at all interfaces leads to the net reflectivity that is a sum of all reflected rays at the front surface of the wafer. As the thickness of the film is smaller than the wavelength, film thickness interference arises and the constructive and destructive interference between the rays can affect the net reflectivity. Therefore, the reflectivity of the multilayer film depends not only on the optical properties of the film but it also depends on wavelength and film thickness [117].

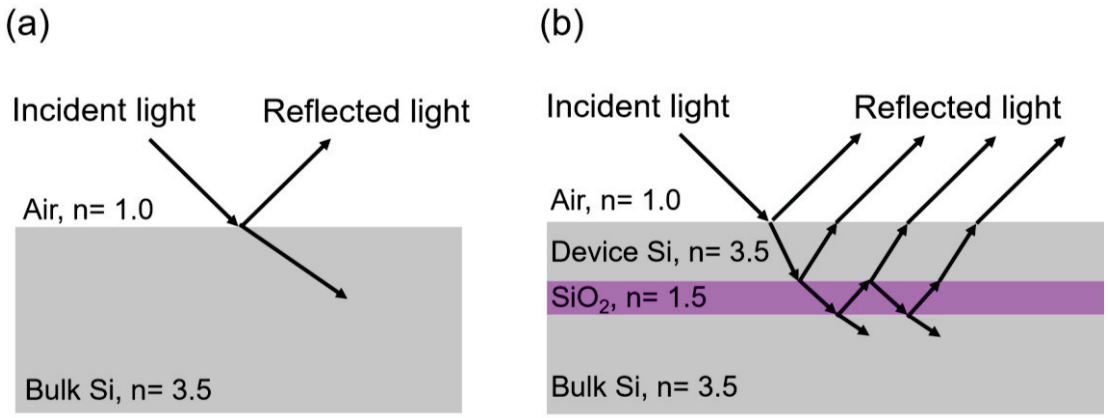


Figure 4.7. Schematic of incident and reflected radiations through (a) bulk Si wafer and (b) SOI wafer.

The coherence length is the distance where the two points are separated along the direction of propagation of the primary light [114]. In this manner, coherence length of light in Si should be taken into consideration. In the simulation, a laser light source with 980 nm has been employed due its high coherence length and Si's reduced absorption

coefficient at this wavelength compared to visible light [12]. The spectral width of the light at our monochromator output of $\Delta\lambda$ ~7 nm at a wavelength of 980 nm corresponds to a coherence length $\lambda^2/\Delta\lambda$ of ~120 μm in free space [114]. However, in Si, where the coherence length is inversely proportional to the refractive index of Si, n, the coherence length is further reduced to ~35 μm in the Si substrate due to the higher refractive index (n_{Si}= 3.50) [12]. The coherence length value can be also calculated as ~25 μm for λ= 800 nm. Comparing derived coherence length of the light employed in our setup to the top Si layer thickness of 10 μm implies that light with broad spectral width will lose its coherence after a few reflections within the formed optical microcavity in BOX layer already. This allows multiple light reflections within the top Si layer and probing interference. GSOI device, in which all interfaces between different materials are parallel like, exhibits a strong interference dependence. Constructive and destructive interference effects due to multiple reflections within the optical cavities formed by the active Si layer and the BOX result in an oscillating behavior of the *R* (see Figure 4.6 (b)).

Using the equation 2.20, D^* of GSOI is calculated ~16 x 10^{12} Jones at 660 nm, whereas D^* of GSi exceeds ~25 x 10^{12} Jones at 905 nm as shown in Figure 4.8 (a). On the other hand, the D^* values for GSOI and GSi devices are higher than the values reported in similar works [12, 42] due to the larger active area of PDs. Apparently, GSOI PD has the highest detection limit as well as the GSi under zero bias. Figure 4.8 (b) shows the spectral *NEP* of GSOI and GSi devices which was calculated using the equation 2.21. GSOI and GSi devices exhibit low *NEP* down to 0.035 pW $Hz^{-1/2}$ and 0.02 pW/$Hz^{-1/2}$ at the wavelength of 660 and 905 nm, respectively. This value is lower than that reported in a similar work [12]. The increased dark current of the GSOI device compared to GSi device leads to an increase of the *NEP* value, subsequently, the detectivity decreases. While the *NEP* values GSi can not be varied in the whole spectrum, the *NEP* value of the GSOI increases almost ~5 times towards the near infrared region (λ > 800 nm), respectively. Here, the photoresponse is obtained in the active layer where the incident light is absorbed and remaining light is transmitted into the BOX and handle layer, respectively. However, these parts do not contribute to the photoresponse for longer wavelengths. Additionally, *NEP* values of GSOI change from 0.044 to 0.049 pW $Hz^{-1/2}$ for the wavelength range between 550 and 840 nm. Such small variations in the *NEP* value enable the devices to be operating for a broader bandwidth ranging from visible to NIR spectrum.

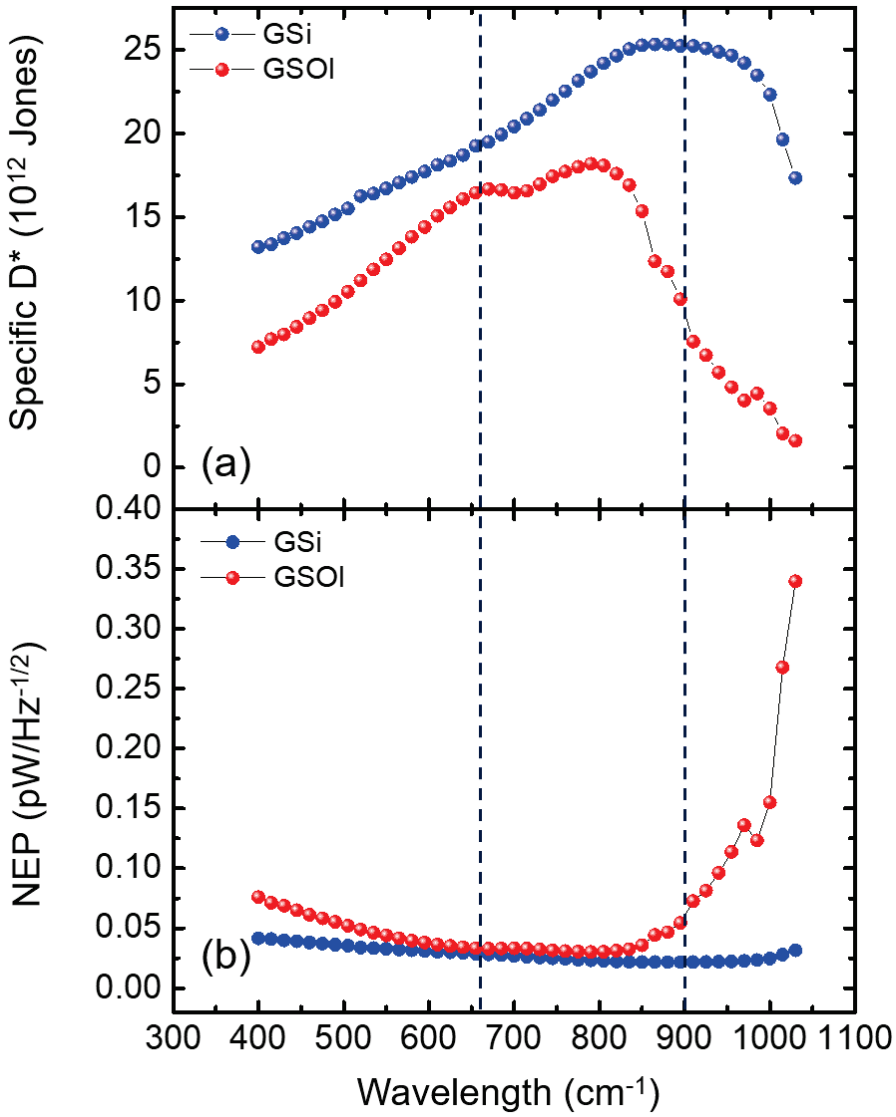


Figure 4.8. (a) Spectral dependence of D^* and (b) *NEP* of the GSi and GSOI devices.

The comparison of the optoelectronic measurement results can be seen in Table 4.1.

Table 4.1. Summary of the performances of single pixel GSOI and GSi based Schottky PDs at 0V bias.

Single-Pixel Device Structure	**Active Area (mm^2)**	**I_{dark} (nA)**	**Response (nm)**	**Rmax (A/W)**	**D^* (10^{12}) (Jones)**	**NEP ($pW/Hz^{-1/2}$)**
GSOI	20	0.9	660	0.52	16	0.035
GSi	20	0.6	905	0.76	35.3	0.013

To conclude, we analyzed the photoresponse characteristics of GSOI Schottky PD and compared these results with the reference GSi PD. We observed that single pixel G/n-Si devices fabricated on SOI and bulk Si showed similar device performances, however,

the R_{max} of GSOI shifted towards lower wavelength due to the decrement in the photoactive Si layer. In general, these results taken from the single pixel provided an idea for the photoresponse characteristics of PDAs. Thus, we decided to take the photoresponse characteristics of the GSi-based PDs fabricated on SOI under 660 nm wavelengths.

4.2. Graphene/SOI-based self-powered Schottky barrier PDA

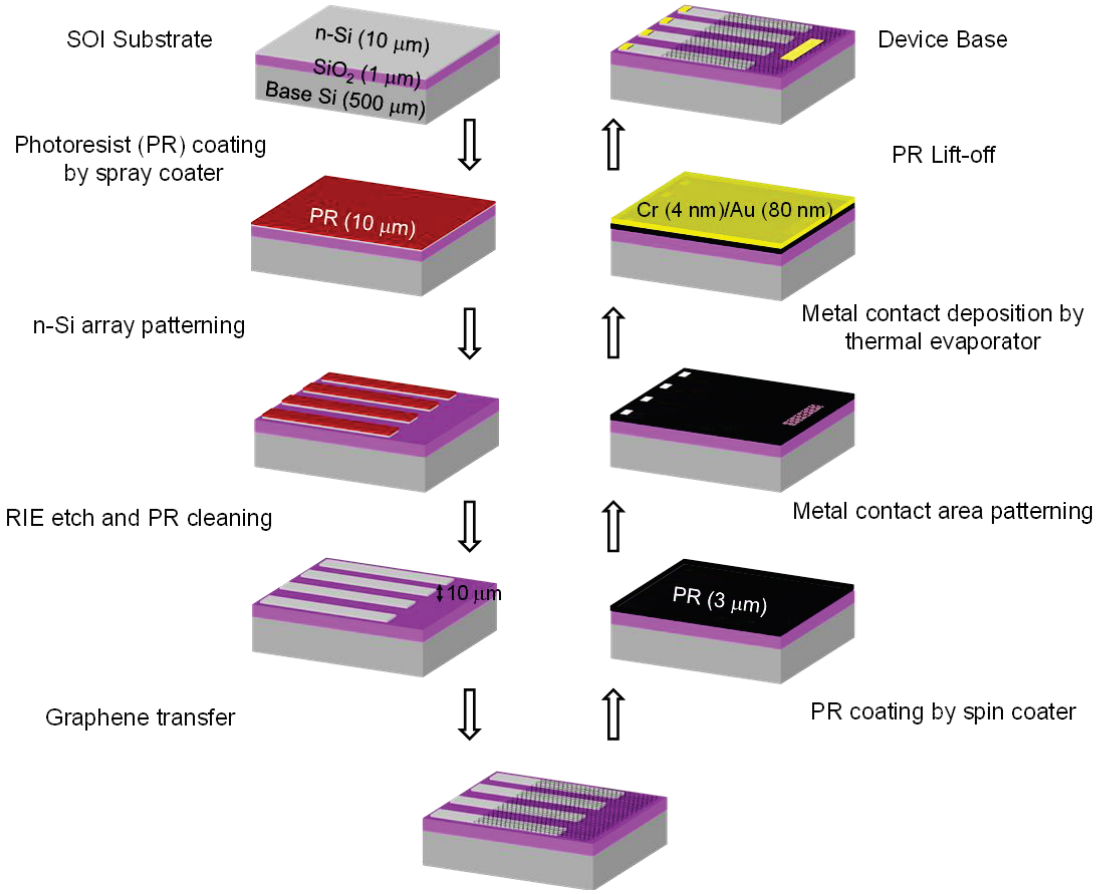
Si-based p-n [118] and/or p-i-n [119] type PDAs are easily accessible in market and well-studied in the literature but there is a main drawback in their working principle that they need external power and high-cost packaging methods. For this reason, it is essential to develop different fabrication methods for Si-based PDAs that require low cost and work in energy-efficiency. G/n-Si heterojunctions have been receiving a great deal of attention in the field of self-powered devices due to ease in fabrication with simple device structure and outstanding device performances [120]. More recently, various methods have been used to fabricate single pixel G/n-Si Schottky devices with different architectures as we discussed in section 2.7. In general, PDA devices are fabricated on bulk Si substrates and one of the drawbacks to obtain G/n-Si PDA on a single Si substrate is the inevitable electrical and optical leakage.

In this section, we demonstrated that a multi-channel G/n-Si Schottky PDA can be fabricated on SOI substrates using standard microfabrication techniques applied in CMOS technology. In our device design, we used the advantage of the BOX layer in SOI, which acts as a well-defined etch-stop and provides an excellent electrical isolation in between laterally aligned neighboring photoactive G/n-Si elements in the array. In the fabrication process, single layer graphene is utilized as a *common* electrode on a linear array of multiple n-type Si channels, which were lithographically exposed on a single SOI substrate. I–V and wavelength resolved photocurrent spectroscopy measurements showed that each G/n-Si element in the PDA operates in the self-powered mode and responds to incident light independent of each other. The optoelectronic device parameters, including spectral R, D^*, NEP, and response speed of the G/n-Si PDA sample, were systematically investigated in this study. The results presented in this section have been published in Ref. [121].

4.2.1. Device fabrication

For the experiments, we used 10 x 10 mm^2 sized SOI substrate which the specifications were given in section 3.1.1. The 4-Element structures were prepared by using maskless lithography as figured out in Figure 3.3 (d) and an array of n-Si channels on SOI substrates was obtained using dry etching method to reach the oxide layer (BOX) layer. Following the fabrication of a Si array, the windows for metal contact pads were defined by an additional lithography step. After the Cr (4 nm)/Au (80 nm) metal contact pads were evaporated both on the n-Si side and on the SiO_2 covered the side of SOI substrates with the thermal evaporation system, the liftoff process was done to obtain our devices. Monolayer G was growth using CVD technique and transferred on the substrate as mentioned in section 3.1.6. Here, CVD grown graphene with a surface coverage of higher than 95% was employed as *common* Schottky electrode and acted as the active region when interfaced with arrayed n-Si substrate. The device fabrication steps can be found in Figure 4.9 (a). The active area of the junction is determined by with the area of 3 mm^2 where Si and graphene meet on arrayed Si. Device dimensions can be seen in Figure 4.9 (b). Each element has a Si dimensions with length and width of 5 mm and 1 mm, respectively. The length between elements is kept constant as 1.5 mm.

(a)



(b)

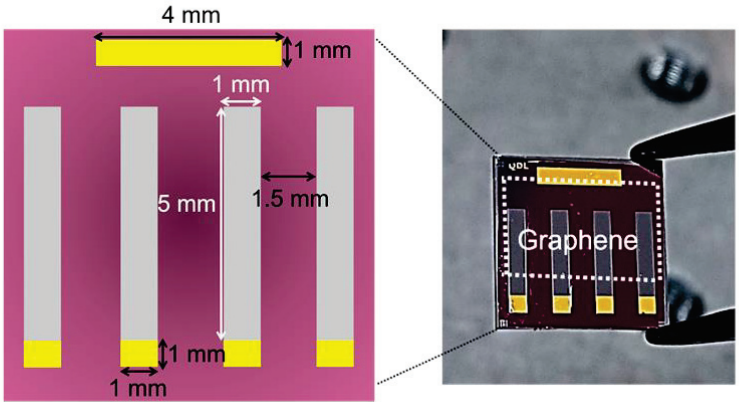


Figure 4.9. (a) Fabrication steps of 4-Element n-Si PDAs with *common* graphene electrode, (b) device dimensions and device picture.

After the transfer process, the presence of graphene on Si and SiO_2 regions of the SOI substrate was determined by single point Raman spectroscopy measurements taken under a laser with 532 nm excitation wavelength. As shown in Figure 4.10, graphene

related D, G, and single Lorentzian shaped 2D peaks were identified in all the obtained Raman spectra. Strong G peak and weak D peak indicate good graphitic quality, and $I_{2D}/I_G > 2$ confirms that graphene is monolayer [107] on the arrayed SOI substrate.

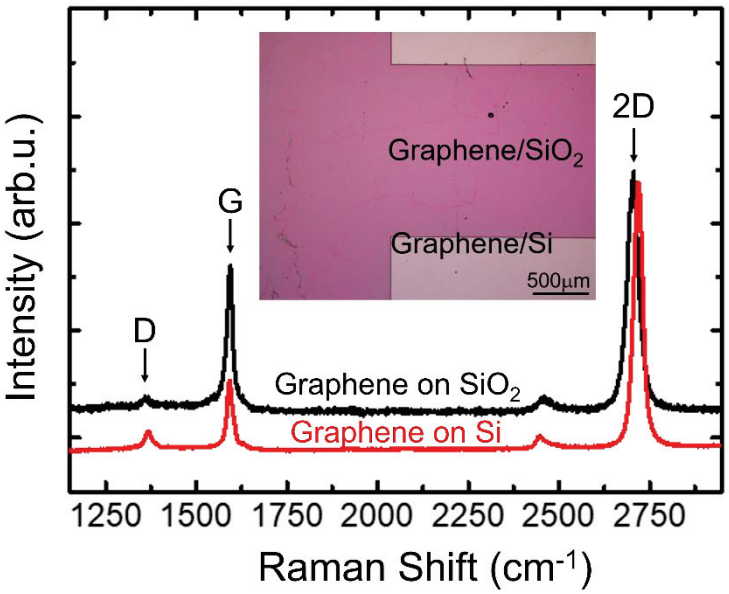


Figure 4.10. Raman spectrum of transferred graphene on Si and SiO_2 sides of SOI substrate (Inset shows the optical micrograph of the region selected for acquiring a Raman spectrum of the graphene layer).

Figure 4.11 (a) shows a schematic illustration of the SOI based four element GSi Schottky PDA fabricated within the scope of this work. Following the Raman analysis, I–V measurements of each G/n-Si element on the SOI substrate were conducted one by one under dark conditions, and the obtained results are plotted in Figure 4.11 (b). All the I–V curves exhibit strong rectifying characteristics of a typical Schottky barrier diode but with slightly different current levels varying in the forward bias region. For a detailed comparison, the I–V data were plotted in the semi-logarithmic scale as shown in Figure 4.11 (c). From the log(I)–V plots, the dark current (I_d) of the G/n-Si elements was extracted as 0.5 nA in average. In the forward bias range, although the current increases linearly at very small voltages in accordance with the well-known thermionic-emission model, the deviation from linearity observed at relatively high voltages (e.g., $V_b > 0.1V$) is due to the series resistance contributions from the underlying n-Si element. The slight difference seen at the reverse bias saturation currents suggests only a small variation in the rectification strength of the G/n-Si heterojunction. Using the equations 2.14 – 2.17 given in section 2.4, the average Φ_B and η of the PD elements were extracted from the

linear forward-bias region of the log(I)–V plot as 0.78 eV and 1.48, respectively. These two diode parameters are consistent with those of GSi based Schottky barrier PDs fabricated on thick and bulk n-Si substrates [94, 122].

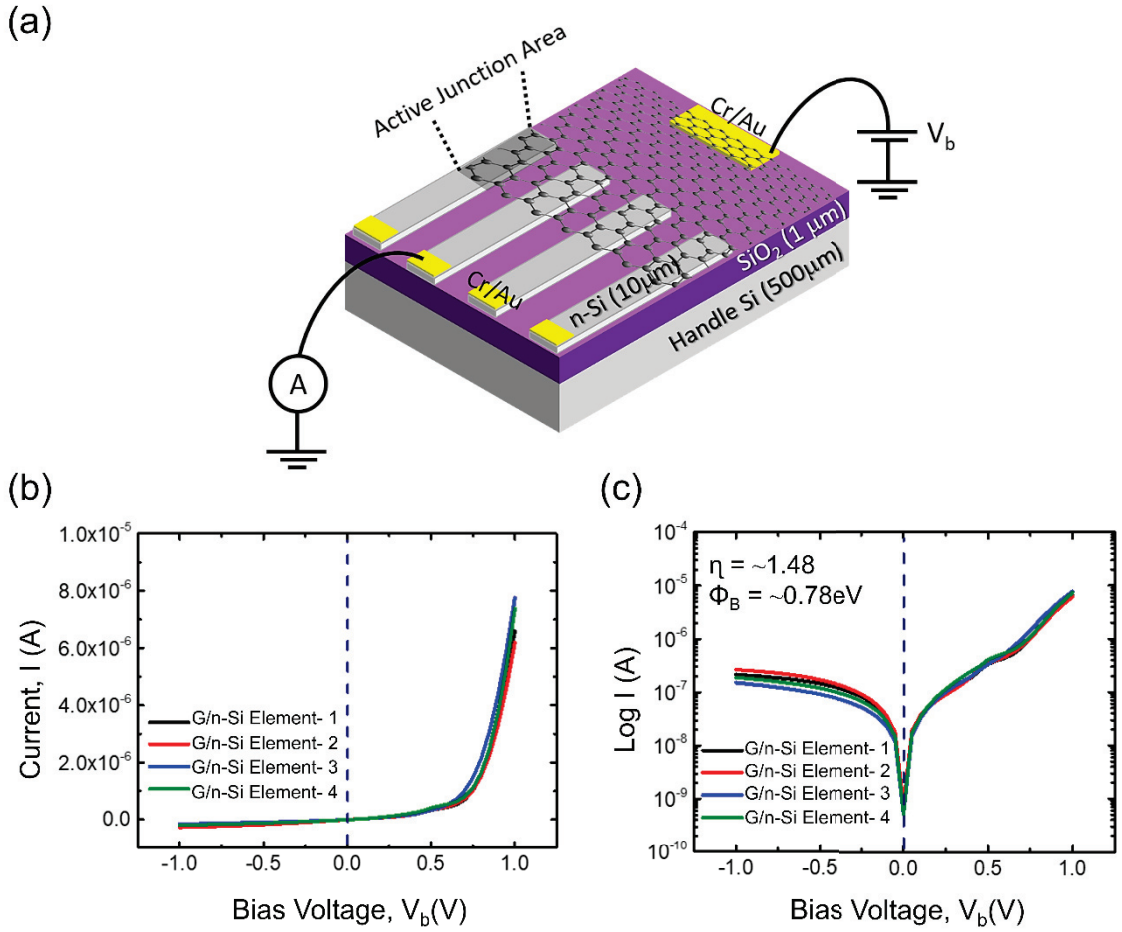


Figure 4.11. (a) The schematic of the fabricated G/n-Si PDA device. (b) The I–V curve of the device in the dark and (c) the log(I)–V plot, which was used to extract the η and Φ_B of each element.

4.2.2. Photoresponse characteristics of the devices

The photoresponse of each individual G/n-Si element in the PDA was characterized separately under illumination of light with 660 nm wavelength. For the experiments, an LED source was coupled to a fiber optic cable with 600 μm core diameter to maintain local illumination on each G/n-Si element and on SiO_2 regions between them as depicted in Figure 4.12 (a). To avoid possible optical crosstalk between neighboring n-Si elements, the distance between the sample and the tip of the fiber optic cable was

kept at 1 mm to ensure well-defined spot size and to minimize possible back reflections that may, respectively, arise from the illuminated Si surface and the metallic tip of the fiber optic probe used in the experiments.

As seen in the log(I)–V plots (Figure 4.12 (c)), all the G/n-Si elements displayed a clear photoresponse with measurable photocurrent (*Isc*) under light illumination even at zero-bias (*Vb* = 0V). The shift of the minimum current seen at the forward bias range corresponds to the open-circuit voltage (*Voc*) and is typical for self-powered G/n-Si PDs operating in the self-powered mode [70]. It is known that, when the G/n-Si heterojunction is subject to light illumination, the incident photons pass through the optically transparent graphene electrode are absorbed by the Si substrate underneath. As a result of photo excitation, electron–hole pairs are created at the depletion region. In the case of zero bias voltage, the depletion region width (X_d) is calculated as 1 μm for a built-in potential (V_{bi}) of 0.7 V and a nominal donor doping concentration (N_d) of $2x10^{15}$ cm^3. The photogenerated charge carriers are separated due to an effective built-in electric field at the interface between the graphene layer and n-Si. Optically excited charge carriers in graphene gain sufficient energy to overcome the Schottky barrier formed at the G/n-Si interface and lead to a photocurrent [123] even at zero-bias (Figure 4.12 (b)). From the I–V plot shown in Figure 4.12 (c), zero-bias I_{SC} of G/n- Si elements was determined to be varying in a range between 1.6 and 3.1 μA under the illumination with 660 nm wavelength light having a power of 380 $\mu W/mm^2$. In the case when the light source is brought on the SiO_2 regions located in between two neighboring active elements (Figure 4.12 (a)), the zero-bias currents of G/n-Si elements were measured as 3.1–9.4 x 10^{-9} A. Compared to the corresponding I_d values, such a slight increase in the measured currents is due to a trace amount of light, which was randomly reflected back from the tip of the metallic casing of the fiber optic probe onto the surface of photoactive G/n-Si elements. When the effects of reflected light on the measured current are ignored, it is possible to state that there is almost no crosstalk between neighboring G/n-Si elements in the array.

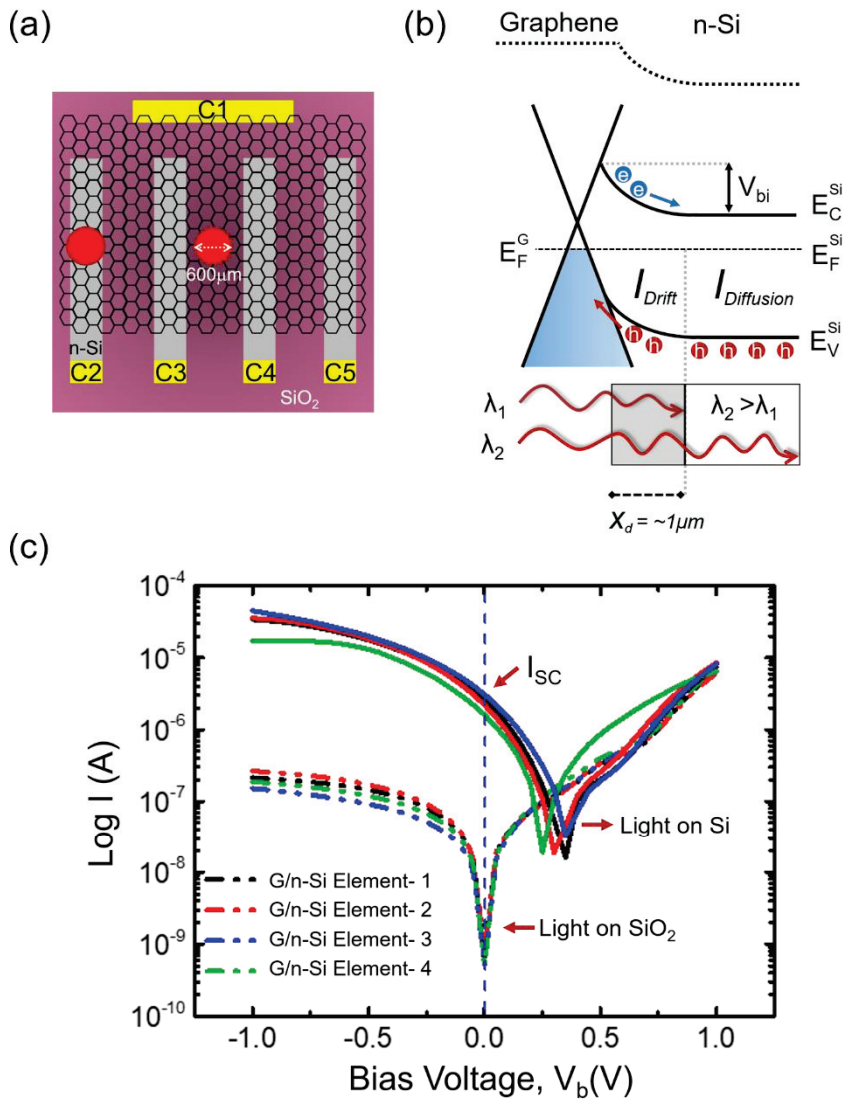


Figure 4.12. Optical crosstalk measurement results of G/n-Si Schottky PDAs: (a) local illumination on each G/n-Si element and illumination on SiO_2 regions located in between two neighboring active elements; (b) the schematic illustration of the energy band diagram for the self-powered G/n-Si Schottky PDAs under light illumination and cross section through the top Si layer, indicating light and optical carrier contributions of drift and diffusion current, I_{drift} and $I_{diffusion}$, respectively; and (c) log(I)–V measurements acquired on G/n-Si elements and on SiO_2 regions between them. (C1: common graphene contact and C2, C3, C4, and C5 represent the contacts on n-Si).

4.2.3. Spectral response

The spectral *R* of each element in the PDA was measured at $V_b = 0$ V as a function of λ of the incident light varied in the spectral range between 400 and 1050 nm. The

obtained results were compared with those of a typical G/n-Si based reference PD fabricated on a 500 μm thick bulk n-Si having the same doping concentration as the n-Si layer on the SOI substrate. *R* values were determined using the equation 2.18. As seen in Figure 4.13 (a), the maximum spectral R_{max} of the reference PD and G/n-Si element with a 10 μm thick active Si layer were determined as ~0.7 AW^{-1} (λ_{Rmax}= 905 nm) and ~0.1 AW^{-1} (λ_{Rmax}= 660 nm), respectively. The difference in the maximum R_{max} is due to the active junction area of the reference PD (20 mm^2), which is larger than that of each G/n-Si element (3 mm^2) in the array. It has been shown that the larger active junction area leads to a wider depletion region, which promotes the effective separation/collection of the photogenerated charge carriers at the depletion region. As a consequence of enhanced charge separation efficiency, I_{SC} and *R* increase proportionally with the size of the active junction area [95]. The blue shift observed in the maximum spectral response wavelength for G/n-Si elements in the array is due to a thin Si layer. Compared to bulk Si, the absorption of light is limited to shorter wavelengths in the case of thin Si layer as discussed in Ref. [124].

For a detailed comparison, normalized spectral R_{max} of the reference PD and a typical G/n-Si element were plotted in Figure 4.13 (b). Different from that of the reference PD, the spectral R_{max} of the G/n-Si element exhibits two maxima located at around 660 and 780 nm wavelengths and decays earlier for the wavelengths above 780 nm. The observed difference in the two distinct spectral R_{max} characteristics can be understood in terms of the penetration depth of light and reduced absorption coefficient of the Si layer on SOI. The photoresponse contribution is only provided by the absorption of incident light in the active thin Si layer on SOI when compared with bulk Si. The BOX layer and Si handle make ineffectively the remaining light power for photoresponse gain in the SOI structure [12]. Accordingly, light-trapping concepts that prolong the light path in thick and bulk Si substrates should be considered. Although only the drift currents contribute in shorter wavelengths, diffusion currents become dominant in a longer wavelength regime where the light penetrates deeper into the substrate (Figure 4.12 (b)). For GSi Schottky PDs on bulk Si, in which the depletion region is wider compared to that of the G/n-Si element out of thin Si, the spectral R_{max} is shifted toward longer wavelengths due to increased amount of the diffusion currents [10]. Because of the fact that the spectral R_{max} of G/n-Si elements in the array appears to decline earlier than that of GSi PD fabricated out of thick and bulk n-Si substrates [125]. As also reported for SOI based single pixel GSi

Schottky PD [12], the photo-active thin Si forms an optical microcavity on the layered structure of the SOI substrate and causes an oscillating spectral R as displayed in Figure 4.13 (b). Such an oscillatory behavior arises from constructive and destructive interference effects due to multiple reflections occurred between different interfaces in the SOI structure[12].

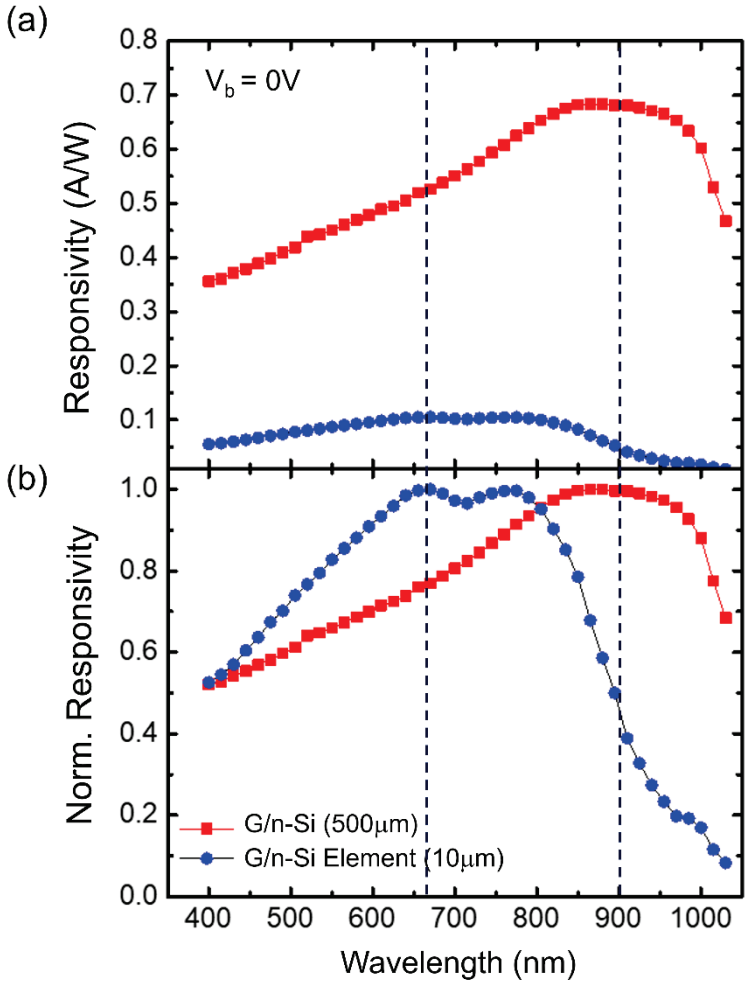


Figure 4.13. (a) Comparison of the spectral R_{max} of a typical G/n-Si element in the PDA device on the SOI substrate (blue) and a reference GSi Schottky PD fabricated on a 500 μm thick bulk Si substrate (red) under zero-bias voltage. (b) Comparison of the normalized spectral R_{max} of these two devices.

Taking into account the R_{max} read at 660 nm wavelength, we also calculated the D^* and *NEP* parameters of each active element in the array by using the equations 2.20 and 2.21, respectively. Considering R_{max} = 0.1 AW^{-1} and A = 3 mm^2, the average D^* and *NEP* of the G/n-Si elements were calculated as ~1.3 × 10^{12} Jones and ~0.14 $pW/Hz^{-1/2}$,

respectively. These two PD parameters are in good agreement with those of both single pixel GSi PD on SOI and GSi PD on bulk Si substrates [12, 126].

4.2.4. Time-resolved photocurrent spectroscopy results

In order to determine the response speed and 3-dB B_w of the active elements in the PDA, we conducted time-resolved photocurrent spectroscopy measurements using the experimental set-up illustrated in Figure 3.15. The measurements revealed that all the elements have excellent photocurrent on/off reversibility as seen in Figure 4.14 (a). Rise time (t_r) and decay time (t_d) of each individual element in the array were determined from single pulse response measurements taken under 660 nm wavelength light pulsed with 1 kHz frequency. Here t_r is defined as the range that the photocurrent rises from 10 to 90 % of its maximum and t_d is defined similarly. A typical example for single pulse response measurement on an individual G/n-Si element is shown in Figure 4.14 (b). Considering the measurements taken on other individual G/n-Si elements in the PDA, the average t_r and t_d were determined as ~1.36 μs and ~1.27 μs, respectively. Using the relation $B_w = 0.35/t_r$, the average 3-dB B_w of the G/n-Si elements in the array was calculated as ~257 kHz.

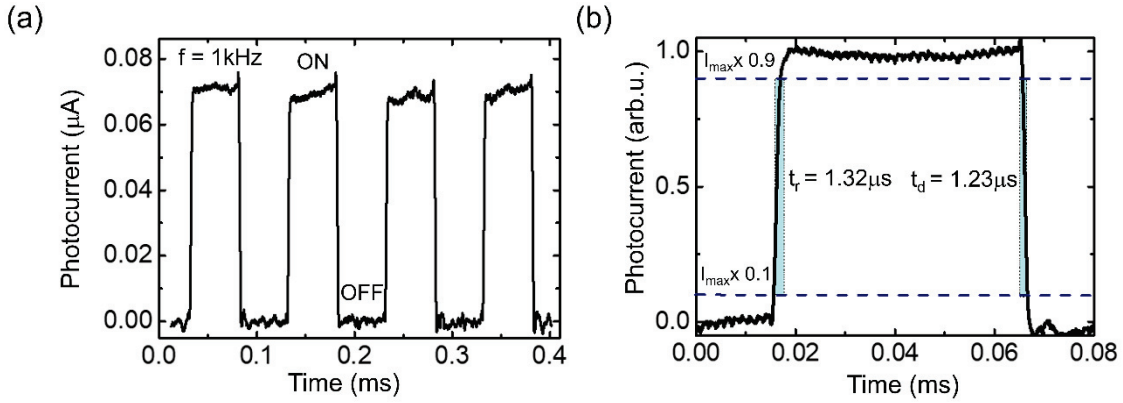


Figure 4.14. (a) Time-resolved photocurrent spectrum of an individual G/n-Si element under 660 nm wavelength light with 1 kHz switching frequency at zero-bias voltage. (b) One cycle time-resolved photocurrent spectrum of an individual G/n-Si element in the PDA device.

For convenience, all the obtained performance characteristics of each element in the PDA device structure are listed in Table 4.2.

Table 4.2. Summary of the performance parameters for four-element G/n-Si Schottky PDAs under 660 nm wavelength light at 0 V bias voltage (junction area, 3 mm^2).

Element ID	I_{dark} (nA)	Rmax (A/W)	D^* (10^{12}) (Jones)	NEP ($pW/Hz^{-1/2}$)	t_r (µs)	t_d (µs)	3-dB B_w (kHz)
G/n-Si Element -1	0.6	0.11	1.38	0.125	1.40	1.28	250
G/n-Si Element -2	0.8	0.10	1.29	0.161	1.38	1.31	253
G/n-Si Element -3	0.5	0.10	1.26	0.127	1.32	1.23	265
G/n-Si Element -4	0.3	0.09	1.25	0.138	1.33	1.21	263

4.3. Self-powered PDA on individual graphene electrode and silicon-on-insulator integration

In order to further minimize the possible optical crosstalk between elements and hence decrease the dark current in junction, it has become important to separate and disconnected individual graphene electrodes on every single Si element in the array and examine the device performances. It is known from the literature that soft patterning method [26] or inject printing method [27] were developed to obtain disconnected and separated graphene electrodes on arrayed substrates. However, these methods require relatively cost effectiveness in their fabrication route. An example was proposed by Grillo et al.[27]. They fabricated the four parallel graphene ink/Si based arrays on commercial heavily doped Si substrate using 'scratch and print' approach. In that study, Si is used as *common* electrode and they faced with the inevitable optical crosstalk effect since photo-generation occurs mainly at the Si surface [28].

As distinct from the literature, we successfully obtained individual graphene electrodes on arrayed Si channels and investigated the optoelectronic characteristics of each element. This section presents the improvement of SOI based G/n-Si Schottky barrier PDAs with separate graphene electrode and hence the elimination of optical crosstalk effect occurred between G/n-Si diodes. The results have also been published in Ref.[127].

4.3.1. Device fabrication

As distinct from our previous work 'G/n-Si PDA with *common* graphene electrode' fabrication route given in section 4.2.1, the device structures were prepared by using three-stage photolithography technique. Large area grown monolayer graphene was transferred on arrayed SOI substrate following the fabrication of Si array and shaped with thick photoresist (t~15μm) using photolithography, subsequently graphene was etched with O_2 plasma to *separate* graphene electrodes. Following the graphene etching procedure, the windows for metal contact pads were defined by an additional lithography step on individually separated elements. After contact metals were evaporated both on the n-Si channel side and on the G/SiO_2 side of the SOI substrates with a thermal evaporator and then a lift-off process was applied to obtain individual 1D array device structure. A schematic illustration of the experimental process to fabricate the G/n-Si PDA device with active junction area of 3 mm^2 is displayed in Figure 4.15.

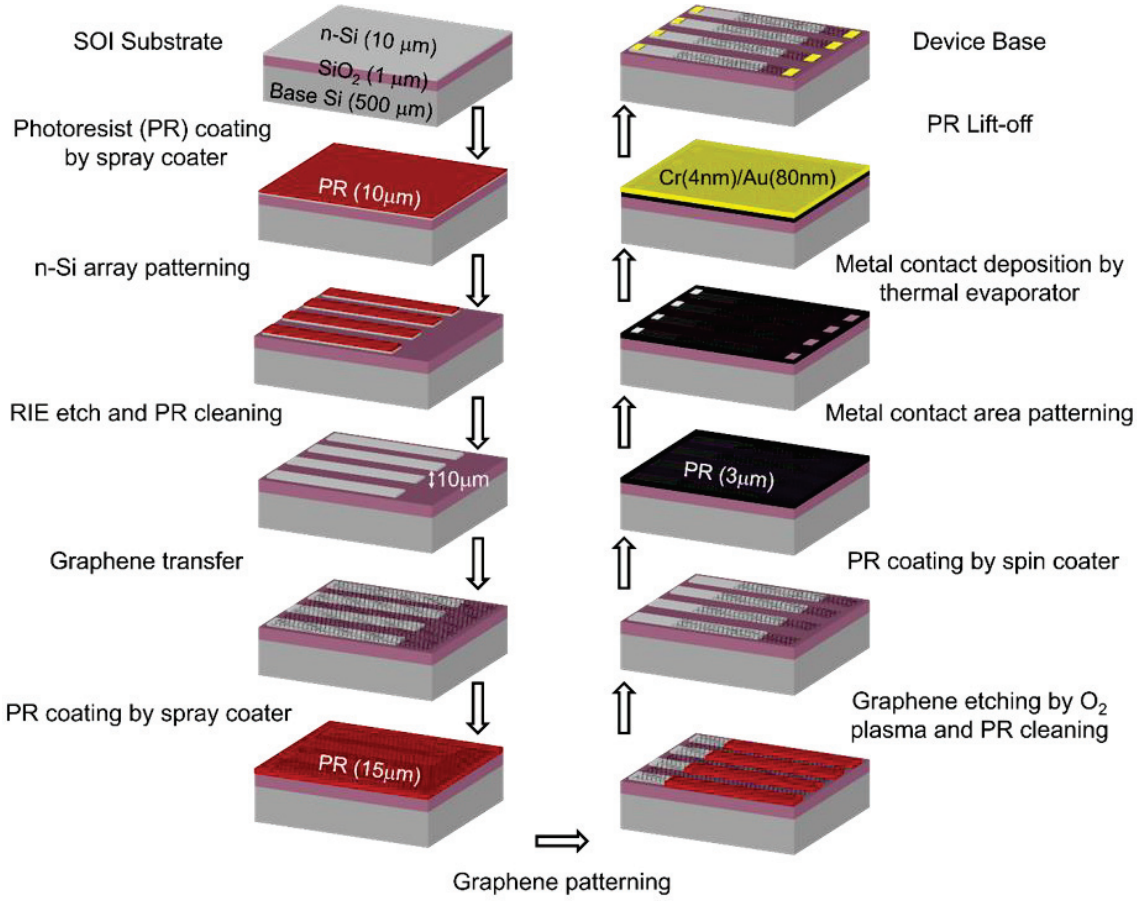


Figure 4.15. Fabrication steps of 4-Element G/n-Si PDAs device base, followed by transferring and individually patterning graphene on SOI.

4.3.2. Characterization of the G/n-Si diode arrays

A cross-sectional view, schematic representation of the individually fabricated 4-element GSi Schottky PDA and optical micrograph taken on diode is displayed in Figure 4.16 (a-c), respectively. After the transfer process, the quality and number of graphene layers on randomly selected spots on the diode surface was determined by single point Raman spectroscopy measurements. Raman signals were recorded in a spectral range between 1200 cm^{-1} and 3050 cm^{-1} using an Ar+ ion laser with a 532 nm excitation wavelength laser source was used with a 0.9 μm spot size. In all measurements, graphene-related D, G, and 2D peaks were found at the peak wavelength of around ~1350, ~1602 and ~2685 cm^{-1}, respectively and well resolved as shown in Figure 4.16 (d). Strong G peak and weak D peak indicate good graphitic quality, and $I_{2D}/I_G > 2$ confirms that transferred CVD graphene is single layer on the device structure [107]. Prior to photocurrent spectroscopy measurements, the I–V measurements of each PD element on the SOI substrate with *separate* graphene electrode were conducted one by one under dark conditions with an applied bias voltage range between −1 and 1 V. All the I-V curves of the diodes displayed typical rectifying Schottky contact behavior which is in good agreement with the TE model [128] given in equation 4.1. Here, A is taken as 0.03 cm^2. From the I–V plots, the dark current (I_d) and saturation current (I_0) values were determined were determined as ~0.4 nA and 2.61×10^{-8} A in average for PD elements, respectively. In the forward-bias range, although the current increases linearly at very small voltages, the deviation from linearity observed at relatively high voltages is due to the series resistance contributions from the underlying n-Si element. The slight difference seen at the reverse bias saturation currents suggests only a small variation in the rectification strength of the G/n-Si heterojunction. For a detailed comparison, the I–V data were plotted in the semi-logarithmic scale as shown in Figure 4.13 (e). Using the method developed by Cheung et al.[89], the average Φ_B and η of the PD elements with separate graphene electrode were extracted from the linear forward-bias region of the log(I)–V plot as ~0.81 eV and ~1.51, respectively. Considering the Schottky–Mott model, where Φ_B is defined as the difference between the Φ_G and the χ of Si (χ_{Si} = 4.05 eV), Φ_G was calculated as ~4.86 eV in average for PD elements, respectively. These two diode parameters are consistent with the results in section 4.2.1.

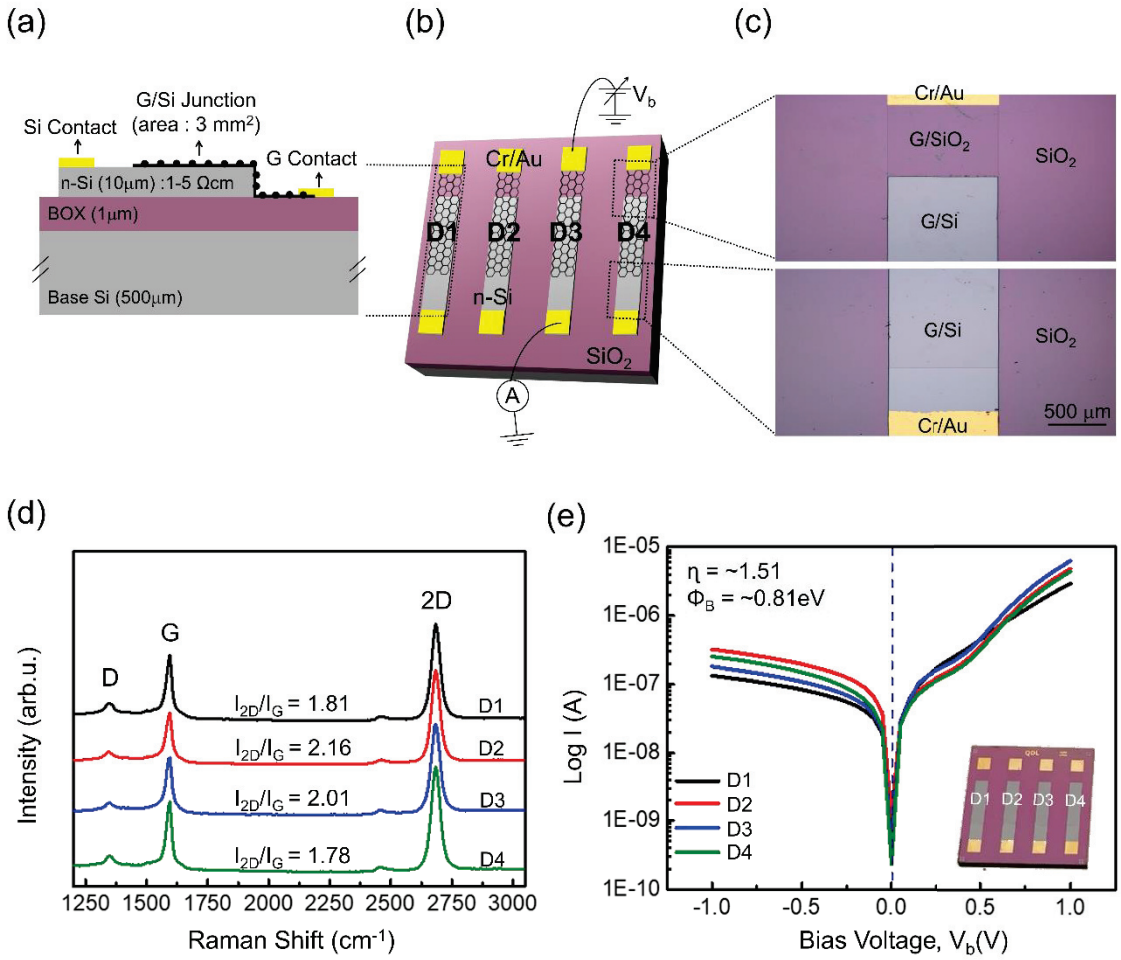


Figure 4.16. (a) The cross-sectional view of the device where graphene is transferred on the planar Si (100) surface and (b) schematic structure of the fabricated individual G/n-Si PDA device (D1, D2, D3, and D4 represent the G/n-Si diodes arrayed on SOI), (c) optical micrograph of the diodes, (d) a typical single-point Raman spectrum taken on randomly selected region of the diodes and (e) the log(I)-V plot of the devices with separate graphene electrode in dark which was used to extract the η and Φ_B of each element. Inset: Device photograph.

4.3.3. Measurement of the optical crosstalk of the G/n-Si diode arrays

For optical crosstalk measurements, we used an LED source with 660 nm wavelength coupled to a fiber optic cable tip with 600 μm core diameter to locally illuminate each individual diodes and SiO_2 regions between them in the PDA. Each diode has a Si dimensions with length and width of 5 mm and 1 mm, respectively. The length between elements is kept constant as 1.5 mm (Figure 4.17 (a)). Firstly, an optical source is provided to only one pair of the anode (n-Si) – cathode (G) electrodes in the individually arrayed PDs where the separate cathode is biased with a certain voltage range

between -1 and 1 V. The distance between the sample and the tip of the fiber optic cable was kept at ~1 mm to ensure a well-defined spot size and avoid possible back reflections that may respectively arise from the illuminated Si surface and the metallic tip of the fiber optic probe used in the experiments. From the log(I)–V plot shown in Figure 4.17 (b), the short-circuit current (I_{SC}) where photocurrent measured at zero-bias were determined to be varying in a range between 4.2 and 7.5 μA. In the case when the light source is brought on the SiO_2 regions located in between two neighboring active elements, the zero-bias currents of diodes were measured as ~5 nA which is more than almost tenfold compared to the corresponding I_d values. As depicted in Figure 4.17 (a) with 4 pairs of electrodes, optical illumination is present on the junction of D2. Subsequently, the generated photocurrent at every other anode-cathode electrode pair (i.e. D1, D3, and D4) is extracted in the same measurement, respectively. The total crosstalk as amplitude in any array can be determined as the total sum of photocurrent at diode I_{Dn} (excluding the illuminated diode) over the photocurrent generated at the illuminated element and can be written as [24];

$$Total\ Crosstalk = 20 * log\left(\frac{I_{D1}+I_{D3}+I_{D4}}{I_{D2}}\right) \quad 4.4$$

where I_{Dn} is the photocurrent that flows at the anode indexed as n = 1,2,3,4 and I_{D2} is the measured photocurrent in diode D2. Therefore, when D2 is illuminated, the possible optical crosstalk at D1 can be calculated with [24]:

$$Crosstalk = 20 * log\left(\frac{I_{D1}}{I_{D2}}\right) \quad 4.5$$

This relation can be generalized to calculate other crosstalk values occurred in other elements. Using equation 4.5, under the illumination of D2 ($I_{SC(0V)}$ = 4.2 μA), we calculated the crosstalk values of -59 dB (0.11 %), -57 dB (0.14 %) and -60 dB (0.10 %) at D1 ($I_{(0V)}$ = 5 nA), D3 ($I_{(0V)}$ = 6 nA) and D4 ($I_{(0V)}$ = 4 nA), respectively. The total crosstalk of -60 dB (0.10 %), -58 dB (0.12 %), -63 dB (0.07 %), and -60 dB (0.10 %) was calculated using equation 4.4 for D1, D2, D3 and D4, respectively. Since each diode is individual from each other, the most important factors for low crosstalk values can be discussed as the constant length between diodes and the constant distance between the sample and the tip of the fiber optic cable in the measurement as summarized in Figure 4.17 (c). Even the optical crosstalk effect is suppressed in our device structure, as the light source moves away from the diodes or the distance between the diodes gets closer,

the possible crosstalk effect will increase due to the limitations in our measurement setup. For all the diodes, we observed similar trend but these small variations in optical crosstalk values can be caused by a trace amount of light which was randomly reflected back from the tip of the metallic casing of the fiber optic probe onto the surface of photoactive G/n-Si elements or due to the yield associated with graphene transfer process. After transfer process, there could be some local defects, cracks or wrinkles which result in unintentionally doping of graphene or some inhomogeneities at the G/n-Si interface. These mechanisms affect the optoelectronic characteristics of the graphene based PDs [95]. The total optical crosstalk value that we obtain in G/n-Si Schottky PDA with *common* graphene electrode was ~0.25 % (-52 dB) where $I_{(0V)}$ = ~6.3 nA and $I_{SC\ (0V)}$ = ~2.4 μA. Here in, we calculated total optical crosstalk value as ~0.10 % (-60 dB) for individual diodes. The reason for obtaining high optical crosstalk in PDA with *common* graphene electrode is that the least resistive path for the holes is the one through the graphene and not the one through the Si substrate. When compared to the device with *common* graphene electrode, the one with disconnected graphene electrodes the magnitude of the optical crosstalk between the diodes was found to be decreased by a factor of 150 %. The comparison of optical crosstalk values for G/n-Si Schottky PDA with *common* and *separate* graphene electrode per array in detail can be found in Table 4.3. Despite these circumstances that we mentioned above, our diode arrays showed extremely low crosstalk when compared with a 2D back-illuminated Si vertical p-i-n PDA with 16 x 16 elements device with pixel pitch of 1 mm, gap size of 200 μm and absorption layer thickness of 50 μm where the obtained crosstalk is 10% (-20 dB) [129], and the 4 channel InGaAs-based vertical p-i-n PDAs with 250 μm pitch which produced an optical crosstalk of -35dB (1.77%) [130]. Here, the determination of pixel pitch is essential because as the distance between electrodes were increased, the total crosstalk decreases for all devices in array. However, larger electrode distances cause the decrement in the speed of the device. As seen in the log(I)–V plots (Figure 4.17 (b)), all diodes exhibited a clear photovoltaic activity with measurable I_{SC} under light illumination. The shift of the minimum current seen at forward bias range (e.g., V_b > 0.25 V) corresponds to the V_{OC} and is consistent with self-powered G/n-Si PD operating in the self-powered mode [70]. It is well-known that, when G/n-Si heterojunction is subject to light illumination, the incident photons pass through the graphene and penetrate into the n-Si substrate to create e-h pairs in the X_d. In the case of zero bias regime, the X_d is calculated between optically transparent graphene

and ~10 μm thick n-Si substrate as 1 μm for a V_{bi} of 0.7 V and a N_d of ~2 × 10^{15} cm^{-3}. Owing to the effective built-in electric field at the interface, measurable photocurrent is generated even at zero-bias. The absorption layer thickness has the most profound effect on the total crosstalk. There is a direct proportion between the absorption layer thickness and the crosstalk, because the probability of e-h diffusion to adjacent electrode pair is less for thin absorption thickness when compared with thicker one. For a thicker absorption layer, e-h can be generated deeper within the substrate and they are prone to diffuse to the neighbor electrodes hence increasing the total crosstalk. For instance, the substrate thickness is very critic for Ge-based ILPP arrays with an absorption thickness of 3 μm that show relatively high crosstalk of -21 dB (8.9 %) [24]. Here, the absorption (depletion) layer thickness in our devices is limited with X_d (1 μm) in self-powered mode. This also supports to gain extremely low crosstalk between individual diodes in the array even the effects of reflected light on the measured current are ignored. The narrower depletion region minimizes the crosstalk effect compared to their counterparts working with external bias. Since the size of our devices is in the range of few millimeters (i.e., the distance between the diodes), the resolution is limited by the size of the LED spot. Indeed, the resolution of each element in PDA could easily be further improved by using a focused laser beam.

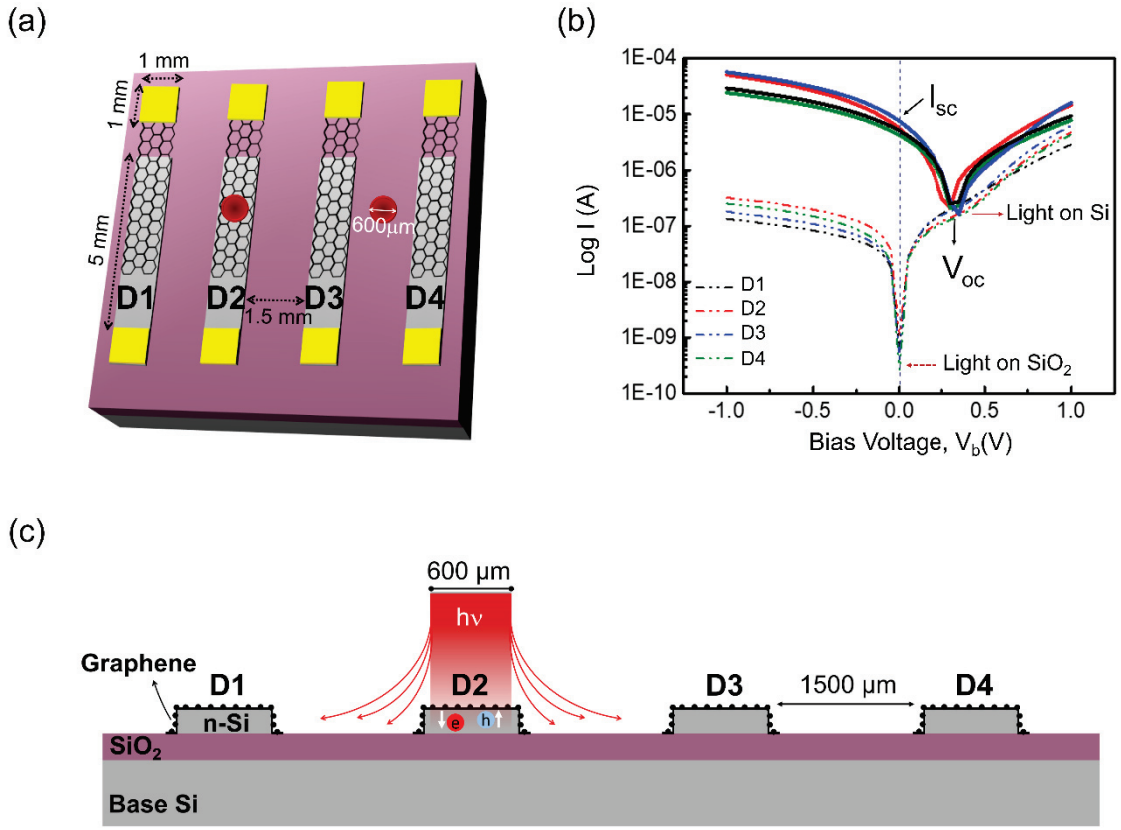


Figure 4.17. Optical crosstalk measurement results of individual G/n-Si Schottky PDAs. (a) Local illumination on each diodes and illumination on SiO_2 regions located in between two neighboring diodes, (b) log(I)–V measurements acquired on diodes and on SiO_2 regions between them and (c) cross-sectional view of possible crosstalk elimination of our device structure. (The diodes were illuminated with 660 nm wavelength light having a power of 380 $\mu W/mm^2$.)

4.3.4. Spectral response

In order to determine the zero-bias R of each element in the PDA, we conducted wavelength-resolved photocurrent spectroscopy measurements under illumination of light in the spectral range between 400 and 1050 nm. The maximum R of the diodes were determined using the equation of 2.18 and observed as ~0.12 AW^{-1} at a peak wavelength of 660 nm and exhibited a decrement towards a cutoff wavelength of 1050 nm due to the band edge of n-Si substrate (Figure 4.18 (a)). The spectral *R* of diodes exhibits two maxima located at around 660 nm and 780 nm wavelengths and decays earlier for the wavelengths above 780 nm. As we explain in section 4.2.3, this phenomena can be understood by the contribution of the drift and diffusion currents, penetration depth of

light and reduced absorption coefficient of Si layer on SOI structure when compared with bulk Si substrate. Besides, the BOX and Si handle layer make ineffective the remaining light power for photoresponse gain in SOI structure [12]. The active Si layer forms an optical microcavity for the G/n-Si Schottky PDA devices and causes an oscillating wavelength dependent *R*. This mechanism is a result of constructive and destructive interference effects by favor of multiple reflections occurred between SOI interfaces.

Taking into account the R_{max} values read at 660 nm wavelength, we also calculated the D^* and *NEP* parameters of each active element in the array. D^* and *NEP* of our samples were calculated using equations 2.20 and 2.21 of section 2.6, respectively and the obtained results were displayed as a function of wavelength in Figure 4.18 (b) and (c), respectively. In agreement with the corresponding R_{max} = ~0.1 AW^{-1} with a junction area of 3 mm^2, the average D^* and minimum *NEP* values were calculated at 660 nm peak wavelength. With D^* = ~1.57 × 10^{12} Jones and *NEP* = ~0.121 $pW/Hz^{-1/2}$, each individual diodes showed similar light sensitivity among diodes with *common* graphene electrode [121] and these results are in good agreement with those of both single pixel GSi PD on SOI [12] and GSi PD on bulk Si substrates [95].

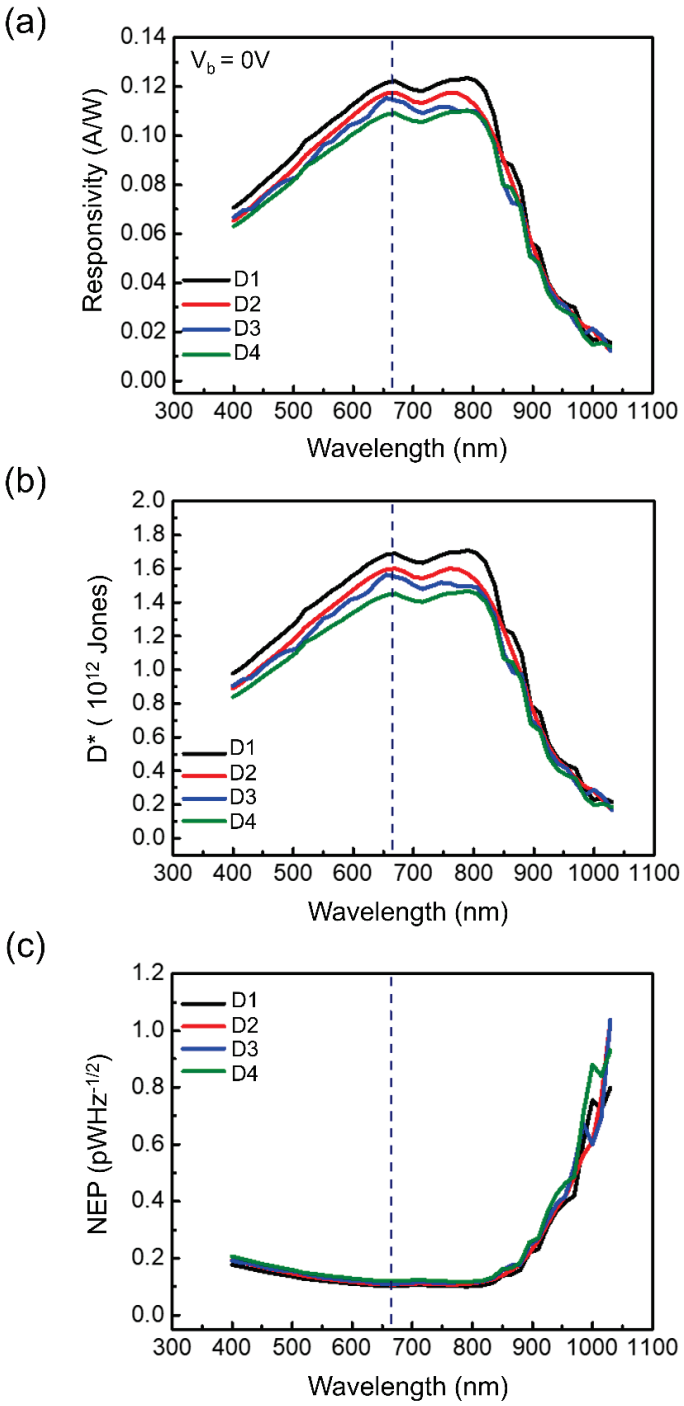


Figure 4.18. (a) The spectral R, (b) D^* and (c) *NEP* of the fabricated individual diodes as a function of wavelength.

4.3.5. Time-resolved photocurrent spectroscopy results

The response speed of the diodes in the PDA were carried out with one-cycle switching on/off within 0.08 ms using time-dependent photocurrent spectroscopy measurements. In the experiments, t_r and t_d of each individual element in the array were

determined from single pulse response measurements taken under 660 nm wavelength light pulses with a frequency of 1 kHz. The measurements were done with the same manner in section 3.3.3 of chapter 3. Here t_r is defined as the range that the photocurrent rises from 10 to 90 % of the peak amplitude output on the leading edge of the pulse and t_d is defined likewise. The measurements revealed that all the elements showed great capability to respond high-frequency pulsed light and on/off switching stability. The single pulse response measurement was done to extract the respond speed of each individual diodes with *separate* graphene electrode as shown Figure 4.19 (a-d). Considering the measurements taken on each elements, the average t_r and t_d were determined as ~1.32 µs and ~1.30 µs respectively. Using the 3-dB B_w relation $B_w = 0.35/t_r$, the average 3-dB B_w of the diodes was calculated as ~266 kHz. For convenience, all performance parameters of each diode in the PDA are listed and compared with our previous study and among themselves in Table 4.3 in detail.

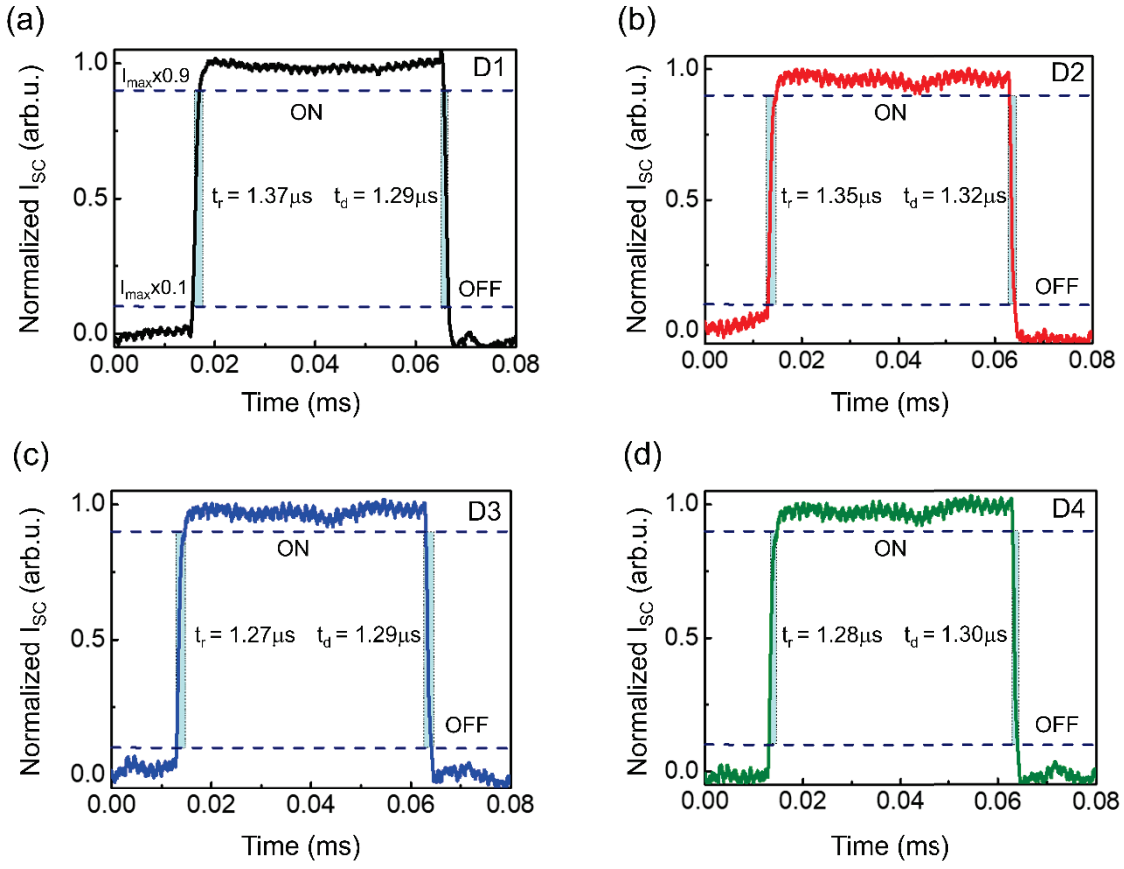


Figure 4.19. The one cycle time-resolved photocurrent spectrum of an individual diodes under 660 nm wavelength light with 1 kHz switching frequency at zero-bias voltage; depending on the element name (a) D1, (b) D2, (c) D3 and (d) D4, respectively. The measured photocurrents were normalized with the maximum values.

Table 4.3. Summary of the comparison of device performances of the diodes under 660 nm wavelength light at self-powered (0 V) operational mode. (Junction area: 3 mm^2).

PDA Device Structure	Diode ID	I_{dark} (nA)	Rmax (A/W)	$D^*(10^{12})$ (Jones)	NEP ($pW/Hz^{-1/2}$)	t_r / t_d (µs)	3-dB B_w (kHz)	Optical Crosstalk (%)
Common Graphene Electrode	D1	0.6	0.11	1.38	0.125	1.40/1.28	250	0.25
	D2	0.8	0.10	1.29	0.161	1.38/1.31	253	0.28
	D3	0.5	0.10	1.26	0.127	1.32/1.23	265	0.26
	D4	0.3	0.09	1.25	0.138	1.33/1.21	263	0.19
Separate Graphene Electrode	D1	0.5	0.12	1.69	0.085	1.37/1.29	255	0.10
	D2	0.9	0.12	1.60	0.142	1.35/1.32	259	0.12
	D3	0.4	0.11	1.56	0.103	1.27/1.29	275	0.07
	D4	0.3	0.11	1.45	0.088	1.28/1.30	273	0.10

4.4. Passive matrix 2D PDA based on graphene/SOI integration

Self-powered 2D passive matrix PDA based on the integration of conventional semiconductors and 2D materials is thought to attract great of interest in the area of image sensing due to energy-efficiency and its ease of fabrication.

After observing the extremely low crosstalk between individual graphene electrodes on arrayed Si channels, we presented the integration of graphene and SOI technology to fabricate 2D PDA in this section. The integration potential was proposed with a 16 pixel of G/n-Si PDs operated with high sensitivity under zero bias regime. In this regard, we systematically investigated the optoelectronic characteristics of each pixel and correlated the pixel quality with surface coverage of graphene sheet by micro-Raman mapping. Also, we demonstrated that novel G/n-Si Schottky 2D PDA device on SOI substrate can be used as a passive matrix image sensor.

4.4.1. Device fabrication

The device structures were prepared by using three-stage photolithography technique as mentioned in section 4.3.1. Large area grown monolayer graphene was transferred on arrayed n-Si and shaped with thick photoresist (t~15 μm) using photolithography, subsequently graphene was etched with O_2 plasma to *separate* graphene electrodes and then G/n-Si pixels were obtained. Following the graphene etching procedure, designed as perpendicular to the Si arrays, the windows for metal contact pads were defined by an additional lithography step. After Cr (4 nm)/Au (80 nm) metals were evaporated both on the n-Si channel side and on the G/SiO_2 side of the SOI substrates with a thermal evaporator and then a lift-off process was done to achieve G/n-Si Schottky 2D PDA device structure (see Figure 4.20).

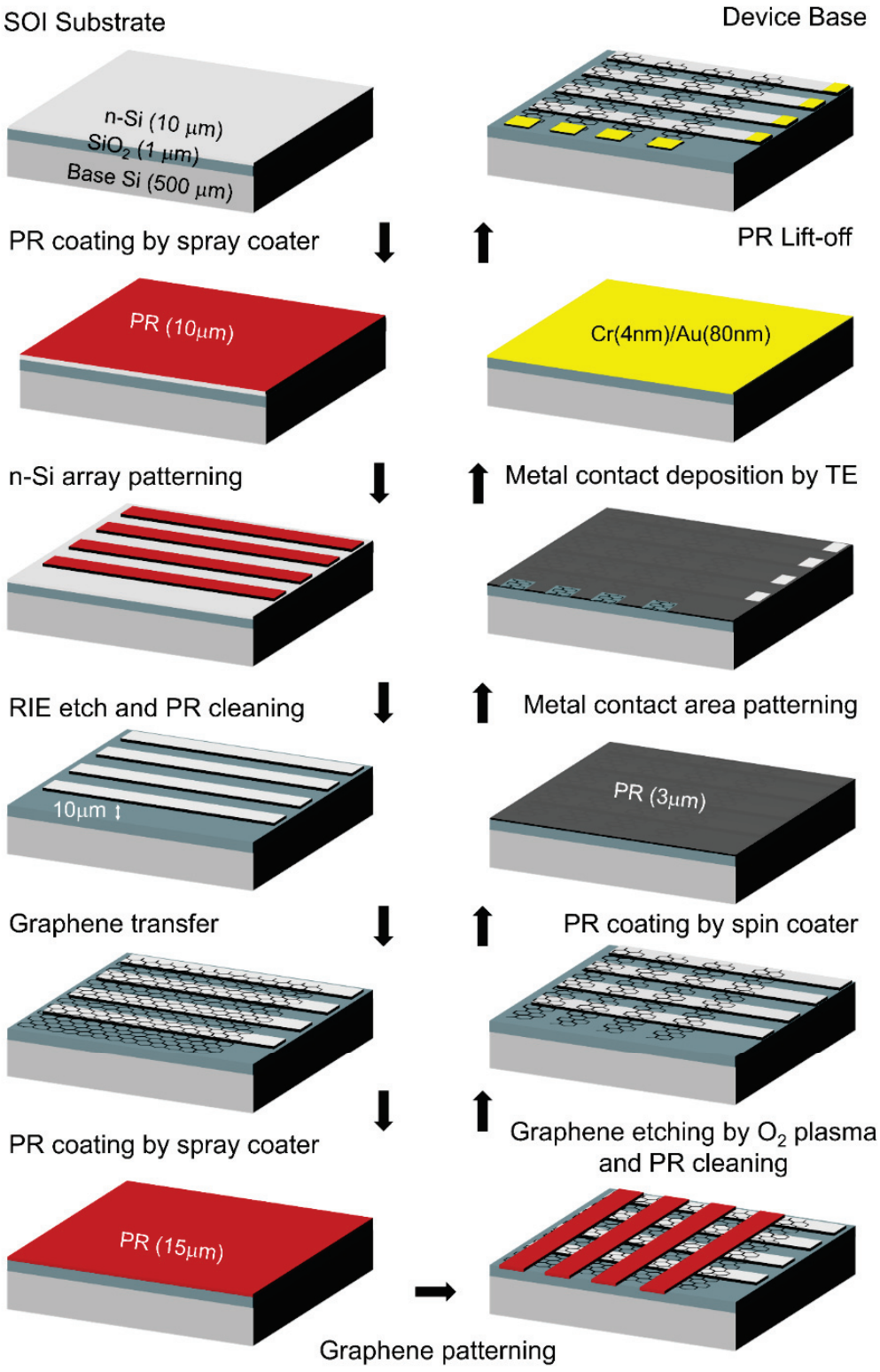


Figure 4.20. Fabrication steps of G/n-Si Schottky 2D PDA device base, followed by patterning n-Si elements, individually patterning of transferred graphene, metallization procedure and device base (The pixel area is 1 mm^2).

4.4.2. Characterization of the G/n-Si pixels

A schematic representation of the fabricated device with electrical contacts is displayed in Figure 4.21 (a). The I–V measurements of each pixel on the SOI substrate were conducted one by one under dark conditions with an applied bias voltage range between −1 and 1 V. All the I-V curves of the G/n-Si pixels displayed typical rectifying Schottky contact behavior and all diode parameters were determined using the TE model [131]. Here, the pixel area where the graphene electrode making direct contact with the n-Si side was 1 mm^2. From the I–V plots, the I_d and I_0 values were determined as ~0.5 nA and 3.93×10^{-8} A in average for pixels, respectively. In the forward-bias range, although the current increases linearly at very small voltages, the deviation from linearity observed at relatively high voltages is due to the series resistance contributions from the underlying n-Si element. The slight difference seen at the reverse bias saturation currents suggests only a small variation in the rectification strength of the G/n-Si heterojunction. For a detailed comparison, the I–V data were plotted in the semi-logarithmic scale as shown in Figure 4.21 (b). Using the method developed by Cheung et al. [89], the average Φ_B and the η of the pixels were extracted from the linear forward-bias region of the log (I)–V plot as 0.82 eV and 1.90, respectively. The reasons of non-ideality for G/n-Si Schottky PDs are known as interfacial oxide layer, interface states, and metallic contaminations due to the fabrication routes of these devices. It is also state that these devices tend to be more ideal by reducing the interface states and the recombination centers inside Si [132]. Considering the Schottky–Mott model, where Φ_B is defined as the difference between the Φ_G and the χ of Si (χ_{Si} = 4.05 eV), Φ_G was calculated as ~4.87 eV in average for G/n-Si pixels, respectively. Each pixel where cathode A, B, C and D in rows and anode 1, 2, 3 and 4 in columns intercept in G/n-Si pixels represents pixel ID in our device structure.

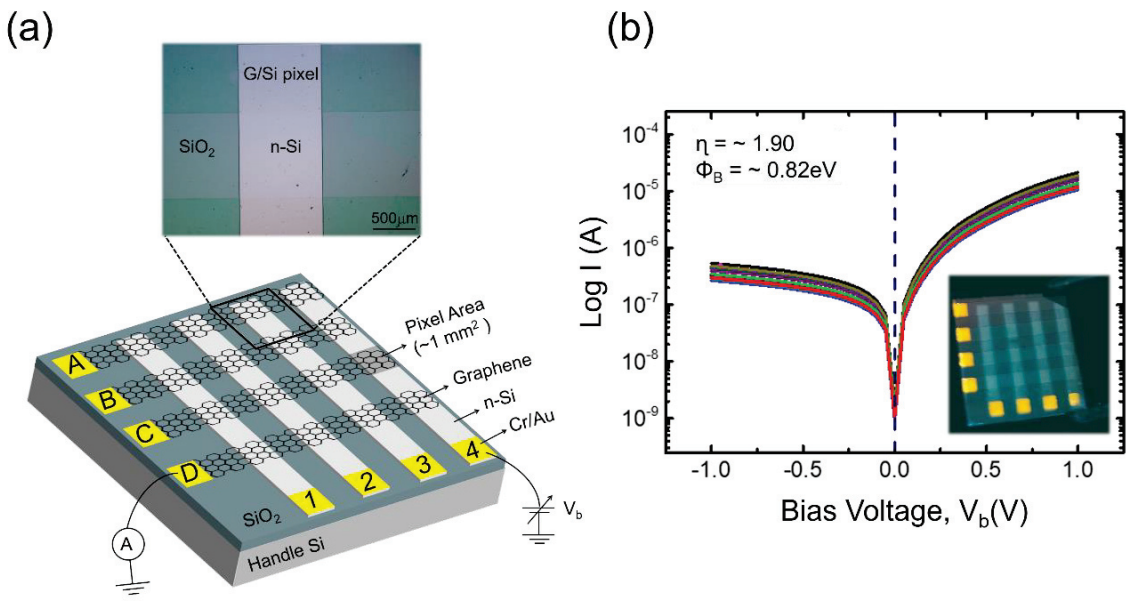


Figure 4.21. (a) The schematic illustration of the fabricated individual G/n-Si Schottky 2D PDAs with device picture and optical microscope image. (b) The log (I)-V plot of the G/n-Si pixels in dark which was used to extract the η and Φ_B of each pixel, respectively (Inset: Device photograph).

Following the I-V measurements, the single-point Raman spectroscopy were performed was performed to determine the number of graphene layers, homogeneity and quality of graphene on randomly selected spots of the D2, B4 and D3 pixel surface. Raman signals were recorded in a spectral range between 1150 cm^{-1} and 2900 cm^{-1}. Raman measurements were repeated several times at different locations on array to ensure continuity. In all the measurements, graphene-related D, G, and 2D peaks were found at the peak wavelength of around ~1365, ~1596 and ~2715 cm^{-1}, respectively and well resolved as shown in Figure 4.22. The 2D peak analyze can be seen as inset of the Raman spectrum of samples. Here, the 2D peak can be fitted with single Lorentzian signal, and the inset figure shows the FWHM value and the R^2 coefficients that give the quality of the fitted experimental data. According to the results, single-layer thickness of the graphene layer was successfully transferred on the arrayed n-Si substrate [107].

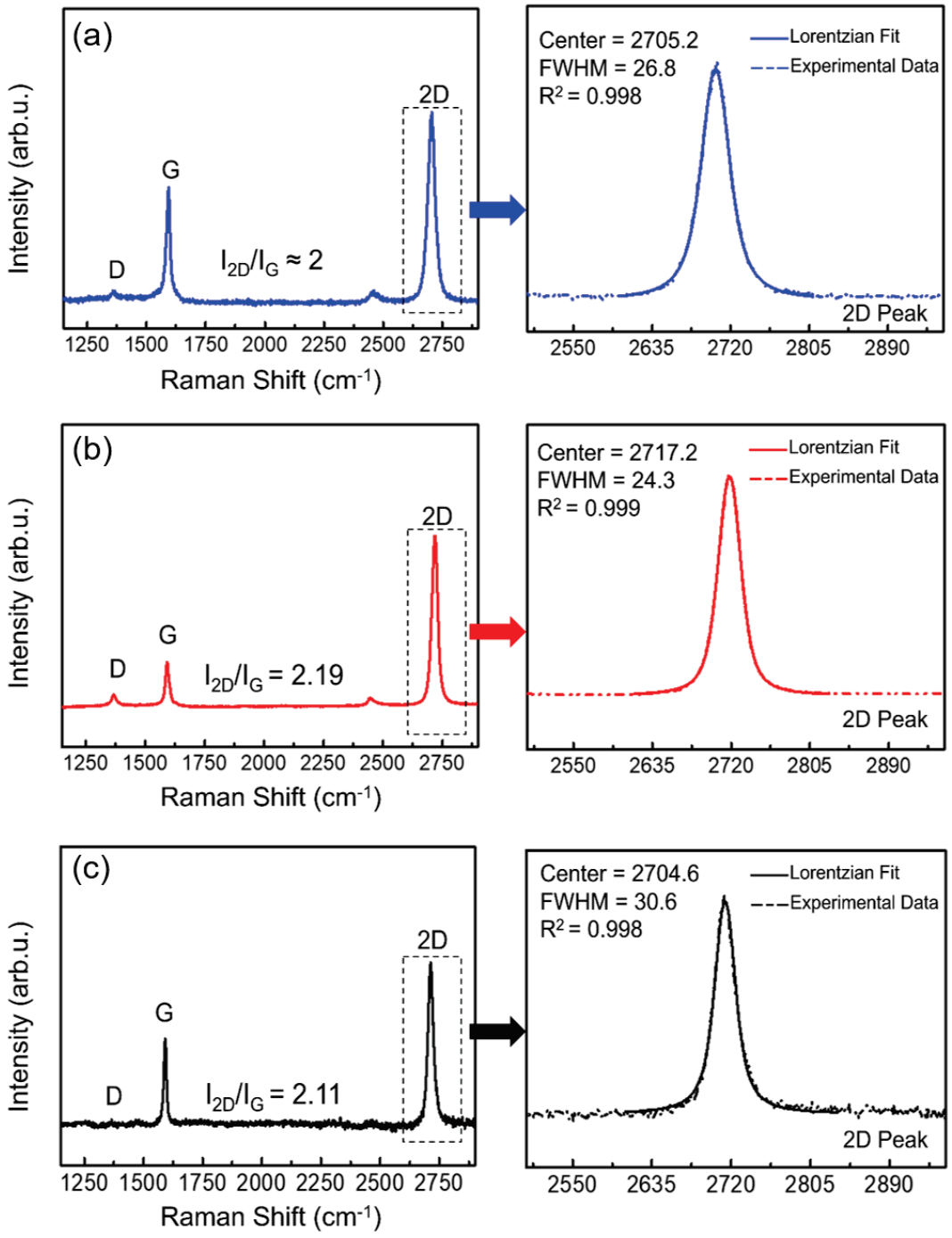


Figure 4.22. A typical single-point Raman spectrum taken on randomly selected region of the pixel (a) D2 (b) B4 and (c) D3, respectively.

4.4.3. Measurement of the optical crosstalk of G/n-Si pixels

For optical crosstalk measurements, we used an LED source with 660 nm wavelength coupled to a fiber optic cable tip with 600 µm core diameter to locally illuminate each G/n-Si pixels, n-Si and G/SiO_2 regions in the device. Here, an optical

source is provided to only one pair of the cathode (G) – anode (n-Si) electrodes in the pixels where the separate anode is biased with a certain voltage range between -1 and 1 V. These procedure was repeated for each pixel. The distance between the sample and the tip of the fiber optic cable was kept at ~1000 μm to ensure a well-defined spot size and avoid possible back reflections that may respectively arise from the illuminated Si surface and the metallic tip of the fiber optic probe used in the experiments. In the case when the light source is brought on the Si and G/SiO_2 regions located in between two neighboring passive pixels (Figure 4.23 (a)), the zero-bias currents of G/n-Si pixel were measured as ~5 nA which is more than almost tenfold higher than I_d values. From the log (I)–V plot shown in Figure 4.23 (b), I_{SC} values were determined to be varying in a range between 3.04 and 9.35 μA. The cross-sectional view of the G/n-Si pixel on the planar Si (100) surface and the schematic illustration of the energy band diagram for the self-powered G/n-Si pixels under light illumination can be seen in Figure 4.23 (c) and (d), respectively.

As mentioned in Ref [18], 2D passive PD matrices are hardly useful for image sensing due to the crosstalk between pixels. In general, this crosstalk makes it difficult to recover information from individual pixels. Here, the determination of size between pixels is very critical because as the distance between electrodes were increased, the total crosstalk decreases as well. However, larger electrode distances cause the decrement in the speed of the device [126]. In our device structure, we kept constant the distance between G and n-Si arrays as ~1 mm and we observed similar trend but small variations in optical crosstalk values due to reflected light back from the tip of the metallic casing of the fiber optic probe onto the surface of photoactive G/n-Si pixels. Accordingly, G/n-Si pixel arrays showed extremely low crosstalk of (~61 dB (0.09%)) when compared with the crosstalk results of the state-of-art Si based ILPP devices [24]. As seen in the log(I)–V plots (Figure 4.23 (b)), all the G/n-Si pixels exhibited a clear photovoltaic activity with measurable I_{SC} under light illumination. The measurable photocurrent can be generated even at zero-bias due to the effective built-in electric field at the G/n-Si interface (Figure 4.23 (d)). It is well-known that, when G/n-Si heterojunction is subject to light illumination, the incident photons pass through the graphene and penetrate into the n-Si substrate to create e-h pairs in the X_d. Under self-power condition, the X_d was calculated as 1 μm and the calculation can be found in section 4.2.3. In our device, the absorption layer thickness in our devices is limited with X_d (1 μm) in self-powered mode. This also

supports to gain extremely low crosstalk between pixels even the effects of reflected light on the measured current are negligible.

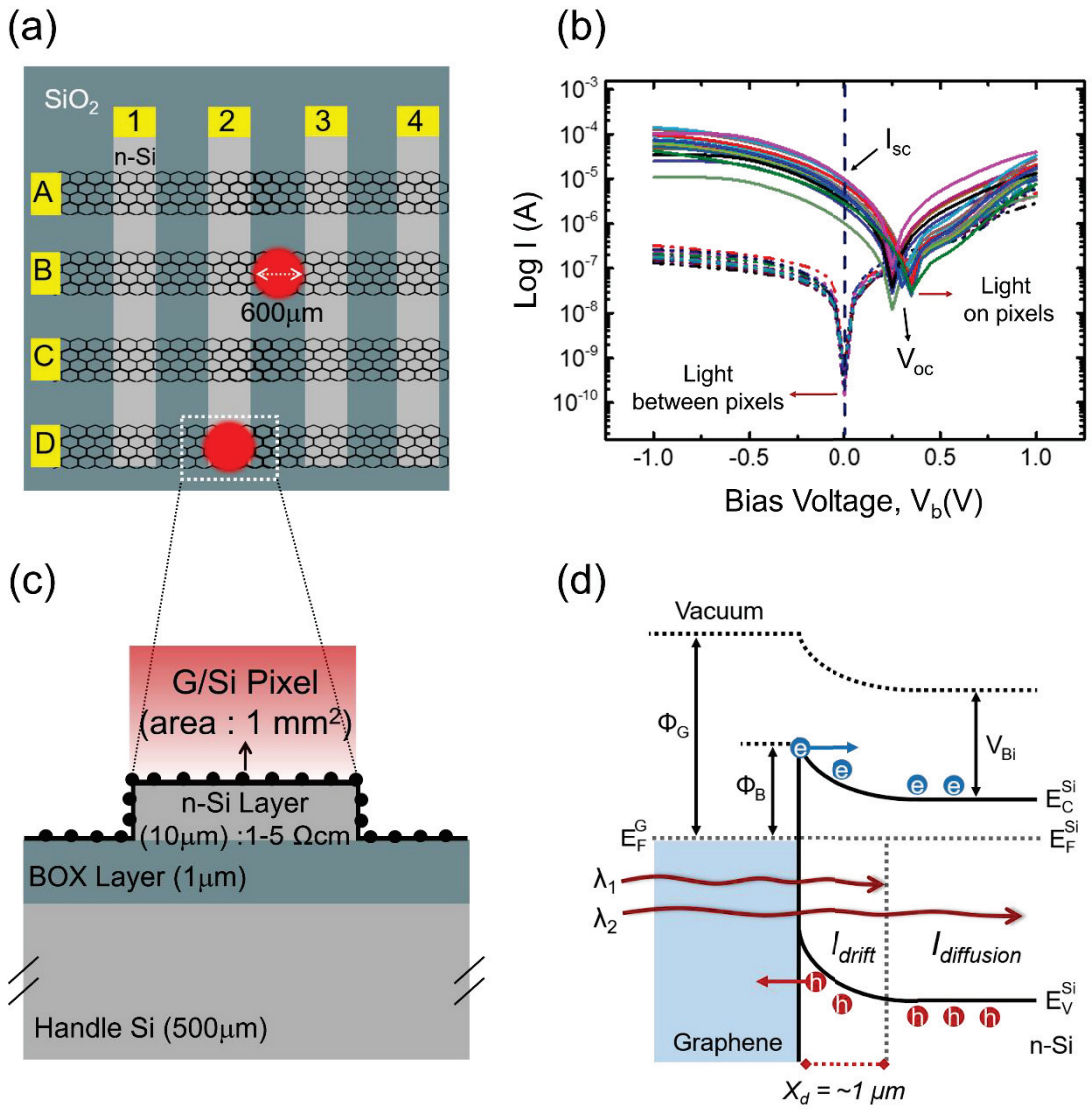


Figure 4.23. Optical crosstalk measurement results of G/n-Si Schottky 2D PDA. (a) Illumination on each G/n-Si pixel with a wavelength of 660 nm and illumination on n-Si and G/SiO_2 regions located in between two neighboring active pixels (the size of the pixels is 1000 μm×1000 μm), (b) log (I)–V measurements acquired on G/n-Si pixel, on n-Si and on G/SiO_2 regions between them, (c) cross-sectional illustration of self-powered G/n-Si pixel and (d) the energy band diagram under light illumination where $\lambda_2 > \lambda_1$ through the top Si layer, indicating I_{drift} and $I_{diffusion}$, respectively.

This new class of optoelectronic device based on G/n-Si heterojunction on a single substrate in 2D array geometry will provide a new design for an image sensor working in the visible spectrum (Figure 4.24 (a)). For this reason, we simulated our device as a passive matrix image sensor with I_{SC} values obtained in optical crosstalk measurement

during scanning in x and y direction. The image sensor consists of an array of G/n-Si PDs with devices in the same row sharing an individual cathode electrode and devices in the same column sharing an individual anode electrode. We encountered the illustration of matrix to image results of a 16 pixel sensor with electrical connections as seen (Figure 4.24 (b)). The rows form the cathode (G) electrodes, and the columns form the anode (n-Si) electrodes. In order to sense the photocurrent of a given G/n-Si pixel, applying local illumination to a row electrode with respect to a column electrode is sufficient to create a photocurrent located at the intersection of the two electrodes.

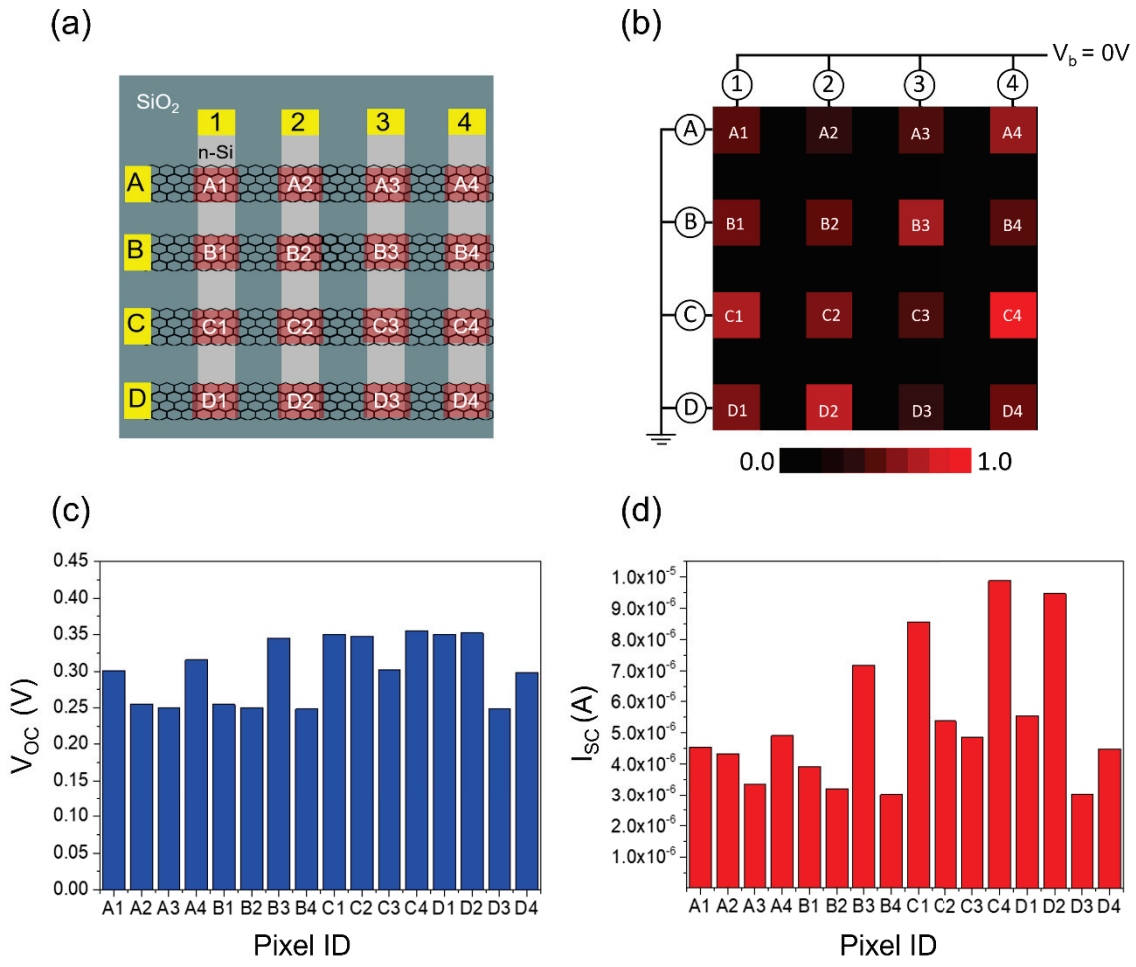


Figure 4.24. (a) Local illumination of each pixel with a constant power density of 380 μW/mm^2, (b) simulation of the passive matrix array device as the image sensor to generate a square pattern with normalized I_{SC} values (c) V_{OC} and (d) I_{SC} histograms of pixels under illumination, respectively.

The pixels shown in red in the image corresponds the active parts where the photocurrent occurs, and the darker regions indicates the regions where there is no G/n-Si junction. The average I_{SC} values were measured as ~6 μA. Despite the distance of

lightning for each pixel are same, we observed that the I_{SC} values at 0 V varied from pixel to pixel. The zero-bias currents measured in the regions in n-Si and G/SiO_2 regions is closer to the I_d values, that's why, these regions are shown as black color in color scale. The zero bias current values obtained in the brighter pixels is in the range of ~3 μA and ~9 μA. Dark red color corresponds to the lowest photocurrent value, and light red color corresponds to high photocurrent value in the color scale (Figure 4.24 (b)). In practice, pixels in the same column and row contribute almost same dark current and photocurrent close to each other. We found that the photoresponse of our G/n-Si Schottky PDs differs from pixel to pixel with same junction area. This is likely caused by the increased number of interface defects in pixel, which can act as carrier trapping centers [126].

For each of the I–V curves, the voltage read at the minimum current and the current at zero-bias correspond to V_{OC} and I_{SC}, respectively. The variation in V_{OC} and I_{SC} for each of the pixels was shown in (Figure 4.24 (c) and (d)). As seen in the corresponding histograms, I_{SC} increases and decreases proportionally depending on the photocurrent value, but the V_{OC} values differ. While I_{SC} increases in some pixels, V_{OC} decreases, while I_{SC} and V_{OC} show linear behavior in some pixels. Consistent with the photoresponse values, the measured I_{SC} had a linear dependence on the junction area [126]. Although the pixel area is the same, such a trend was not observed for the variation in I_{SC} and V_{OC} values. Especially, I_{SC} exhibits a variable response to light at constant power. The nonlinear variation of V_{OC} compared with the I_{SC} is typical for G/n-Si Schottky PDs is explained by the quasi-Fermi level transport model including surface recombination mechanism [133, 134]. As explained by the quasi-Fermi level transport model, V_{OC} generated in a heterojunction device is strongly governed by the magnitude of Φ_B. Therefore, the inconsistent change of V_{OC} with same junction area can be directly associated with the difference in Φ_B of each pixel [126]. Moreover, the charge recombination becomes dominant for light power density about 380 μW/mm^2 throughout the interface states [108].

4.4.4. Raman mapping of G/n-Si pixels

Increase in I_{SC} with the constant light power of 380 μW confirms that the photocurrent in all the samples is solely determined by the amount of photogenerated charge carriers depending on the graphene homogeneity on the pixel. For this reason, we attribute the deformation of the graphene and hence the variation of the junction active

area. To examine the uniformity of the transferred graphene on three different pixels where the low (~3 μA), medium (~6 μA) and high (~9 μA) I_{SC} values were obtained on our device, the intensity to peak ratio of 2D peak mapping was taken over an area of 1000 μm × 1000 μm as shown at the white dashed sides on the substrate (Figure 4.25 (a-c)). The micro-Raman map was acquired in a spectral range between 2550 and 2950 cm^{-1} and the data was recorded for a laser excitation wavelength of 532 nm by raster scanning mode with a precision two-dimensional stage. In the area scan, a 6.5 μm spot size was used with 30 s scan time, five scans per point and 50 μm step size. It should be mentioned that the 2D peak was normalized due to the unintentional weak fluctuations of the laser power during the scanning process [135] which causes small variations in the 2D peak intensity. From the obtained Raman map, the normalized 2D peak variation $\sigma(I_{2D})$ was calculated to be only about 43%, 26% and 19% for lowest, medium and high I_{SC} values, respectively. These plots show an intensity distribution for 2D peak, which further implies the presence of graphene and hence a homogeneous coverage of the graphene throughout the active junction area has an impact of the photosensitive pixel quality.

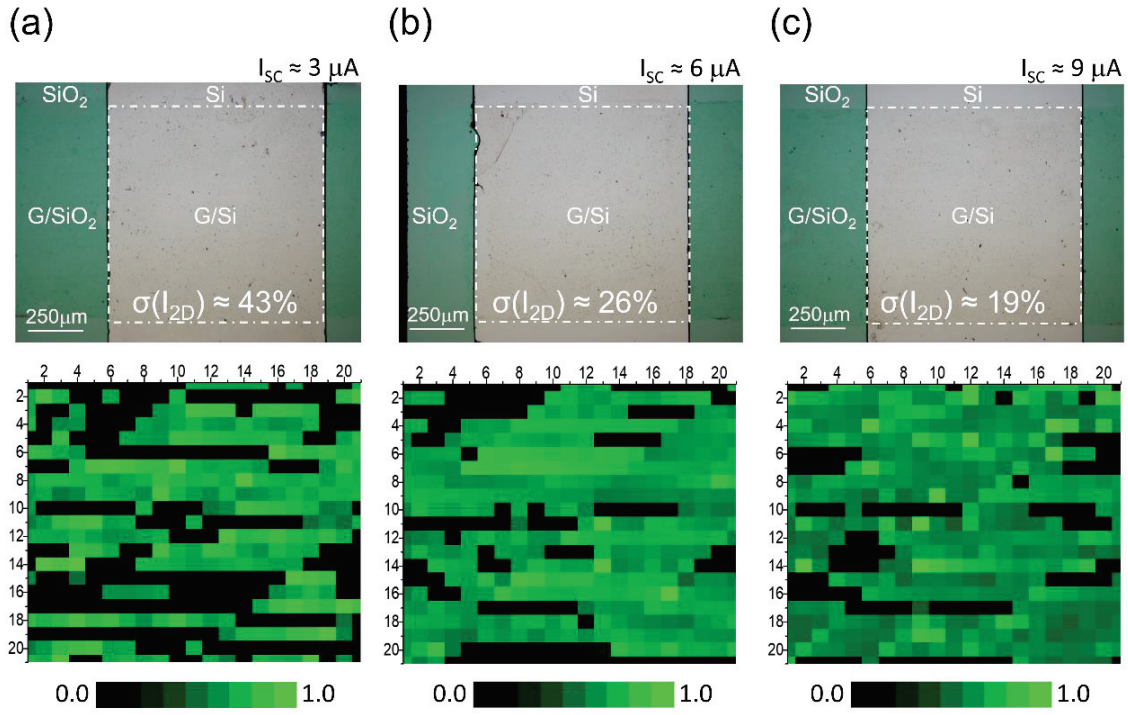


Figure 4.25. Large area integrated 2D peak intensity micro-Raman map of pixel ID (a) D2, (b) B4 and (c) D3, respectively.

The variation in the brightness of pixels is corresponding to the change in the photocurrent observed in each pixel and this situation can be explained as following manner. Since the chemicals used in the graphene growth, transfer and patterning

processes, the fabrication process directly affects the quality of pixels. Even if the graphene is successfully transferred to the sample, there could be some local defects, cracks or residues which causes the unintentionally doping of graphene during the growth and transfer processes (Figure 3.12). Additionally, graphene patterning process can lead the inhomogeneities at the G/n-Si interface. For instance, the developing time is a crucial parameter on this process: in order to minimize the probability for detachment, the developing time must be reduced as much as possible. Due to the small area of the sample, the resist coating might not be uniform, ending up with slightly thicker resist at the edges of the substrate. During the developing in these samples, the resist on the edges might still be present once the structure on the central part of the sample are already well-developed. At this stage, if the sample is kept on the developer for a longer time, the probability for detachment increases. Therefore, graphene sheet can be damaged during this developing time needed for the central part of the sample. In order to improve the photocurrent and hence the R of each pixel, another graphene layer can be transferred on the sample. Transferring an extra graphene layer on the sample can increase the surface coverage of the device and give rise to higher photocurrent values by enhancing the number of photoexcited charge carriers.

4.4.5. Spectral response and time-resolved photocurrent spectroscopy results

We conducted wavelength-resolved photocurrent spectroscopy measurements under illumination of light in the spectral range between 400 and 1050 nm from randomly selected three pixels which have different I_{SC} values on the device in order to determine the zero-bias *R* of G/n-Si Schottky 2D Schottky PDA. The maximum *R* of the G/n-Si pixels were observed as ~0.10 AW^{-1} at a peak wavelength of 660 nm and exhibited a downward trend towards a cutoff wavelength of 1050 nm due to the band edge of n-Si substrate (Figure 4.26 (a)). The spectral *R* of pixels exhibits two maxima located at around 660 nm and 780 nm wavelengths and decays earlier for the wavelengths above 780 nm. As we explain in section 4.2.3, this phenomenon can be explained by the contribution of the drift and diffusion currents, penetration depth of light into the layered structure and reduced absorption coefficient of n-Si layer on SOI. The mechanism can be explained as follows. In a longer wavelength regime, incoming light penetrates deeper into the

substrate. In this case, diffusion currents become dominant compared with drift currents which contribute in shorter wavelengths (Figure 4.23 (d)). The increment in the amount of diffusion currents contributes the photoresponse and shift the spectral *R* toward longer wavelengths in G/n-Si pixel fabricated on bulk Si counterparts. However, the BOX and Si handle layer make ineffective the remaining light power for photoresponse gain in thin Si active layered SOI structure. The active Si layer can also form an optical microcavity and causes an oscillating wavelength dependent *R*. This is a result of constructive and destructive interference effects by favor of multiple reflections occurred between SOI interfaces.

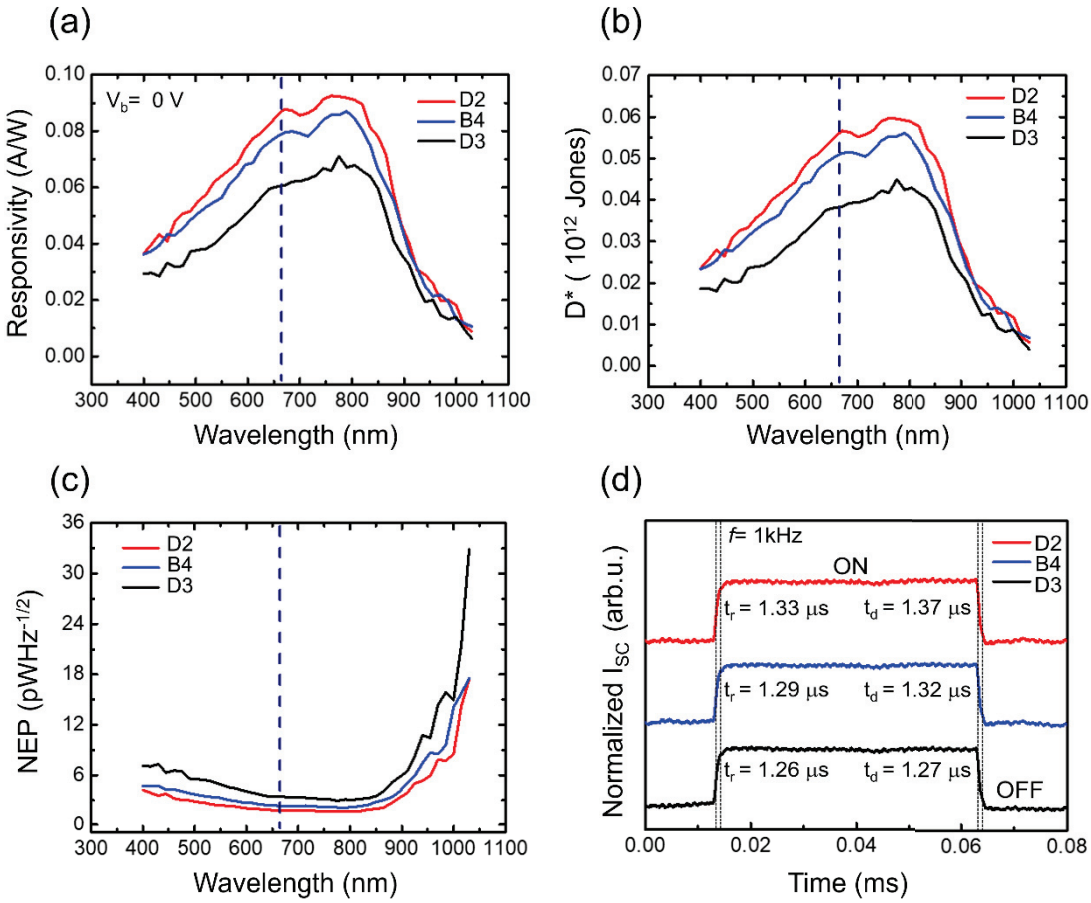


Figure 4.26. (a)The spectral *R*, (b) D^*, (c) *NEP* values as a function of wavelength and (d) one cycle time-resolved photocurrent spectrum of these pixels, i.e. namely D2, B4 and D3, under 660 nm wavelength light with 1 kHz switching frequency at zero-bias voltage. The measured photocurrents were normalized with the maximum values.

Figure 4.26 (b) and (c) represents the calculated and obtained D^* and *NEP* results of our samples as a function of wavelength, respectively. The D^* and *NEP* calculations were done using equations 2.20 and 2.21, respectively. In agreement with the corresponding R_{max} = ~0.08 AW^{-1} with a junction area of 1 mm^2, the average D^* and

minimum *NEP* values were calculated at 660 nm peak wavelength as D^*= ~0.05 × 10^{12} Jones and *NEP* = ~2 pW/$Hz^{-1/2}$, respectively. These results are in good agreement with those of both single pixel GSi PD on SOI substrate [12].

The response speed of the active pixels in the 2D PDA were carried out with one-cycle switching on/off within 0.08 ms using time-dependent photocurrent spectroscopy measurements. In the experiments, t_r and t_d of G/n-Si pixel were determined from single pulse response measurements taken under 660 nm wavelength light pulses with a frequency of 1 kHz. The measurements were done with the same manner in section 3.3.3. The single pulse response measurement were done to extract the respond speed of these pixels as shown in Figure 4.26(d). Although these pixels have different graphene coverage in active area, each pixel revealed great capability to respond high-frequency pulsed light and on/off switching stability. Considering the measurements taken on each pixel, the average t_r and t_d were determined as ~1.29 μs and ~1.32 μs respectively. Using the relation $B_w = 0.35/t_r$, the average 3-dB B_w of the G/n-Si pixel was calculated as ~269 kHz, respectively. Since the graphene coverage is not homogenous in all pixels, the response speed of devices differs from pixel to pixel due to the interface defects. These defects act as carrier trapping centers and alter the on/off performance of PDs.

The comparison of key parameters obtained in our devices with previously reported graphene/Si based PDs fabricated on SOI structure is listed in Table 4.4.

Table 4.4. The photoresponse properties of our device with recently developed G/n-Si based PDs.

Types of Devices	**Junction Area**	**Responsivity**	**Detectivity**	**Rise/Decay Time**	**Refs**
G/SOI in conductor mode	-	10^{17} A/W (V_b = -30 V; λ = 532 nm)	1.46×10^{13} Jones	90 μs/-	[136]
G/SOI	16 mm^2	0.26 A/W (V_b = -2 V; λ = 635 nm)	7.83×10^{10} Jones	~10 ns /20-70 ns	[12]
3D-G/SOI	-	27.4 A/W (V_b = -0.5 V; λ = 1550 nm)	1.37×10^{11} Jones	212μs /242μs	[137]
4-Element G/n-Si Schottky PDA (Common G Electrode)	3 mm^2	0.10 A/W (V_b = 0 V; λ = 660 nm)	1.3x10^{12} Jones	~1.36 μs /~1.27 μs	Our Work (Sec.4.2)
4-Element G/n-Si Schottky PDA (Separate G Electrode)	3 mm^2	0.12 A/W (Vb = 0 V; λ = 660 nm)	1.57x10^{12} Jones	~1.32 μs /~1.30 μs	Our Work (Sec.4.3)
G/n-Si Schottky 2D PDA	1 mm^2	0.08 A/W (V_b = 0 V; λ = 660 nm)	5x10^{10} Jones	~1.29 μs /~1.32 μs	Our work (Sec.4.4)

CHAPTER 5

CONCLUSION

This thesis is focused on the fabrication of self-powered 1D and 2D PDAs based on G and SOI integration. Devices were fabricated by using microfabrication techniques and transferring CVD grown monolayer graphene onto n-Si substrates. The electrical and optoelectronic measurements were performed to determine typical diode characteristics such as SBH, η, spectral R and response speed etc. for each G/n-Si diode. The I-V measurement of the devices in dark environment revealed an excellent typical rectifying character of Schottky diode. The spectral response measurements of G/n-Si diodes in PDAs were done in the wavelength range between 400 nm and 1100 nm. For all the samples, the spectral response exhibited two maxima located at around 660 and 780 nm wavelengths and decays earlier for the wavelengths above 780 nm. The observed difference in the two distinct spectral R characteristics can be understood in terms of the penetration depth of light and reduced absorption coefficient of the Si layer on SOI was measured at a peak wavelength of 660 nm. Afterwards, I-V measurements under the illumination of 660 nm wavelength light were carried out to get photocurrent values of the devices and also determined the possible optical crosstalk between each neighboring diode. All devices showed clear photovoltaic activity and almost negligible low crosstalk value under light illumination. Based on the experimental findings, photoresponse mechanism of single pixel GSOI diode was examined by comparing the device performances with a reference single pixel GSi diode and these results were given in section 4.1 Subsequently, some critical approaches were employed to fabricate GSOI based 1D and 2D PDA devices and the experimental findings were discussed in section 4.2, section 4.3 and section 4.4 in detail. The results of the experiments were summarized in following.

In section 4.1, we systematically investigated the optoelectronic characteristics such as R, D^* and NEP of single pixel G/n-Si Schottky PD on SOI substrate and compared its device performance with a reference GSi PD fabricated on bulk Si to understand the photoresponse mechanism. In this regard, we used bare n-doped photo-active Si (n-Si (100)) layer with the same specifications and also active junction area in each PD was

kept constant as 20 mm^2 for both SOI and bulk Si substrates in order to see the effect of the photoactive layer thickness on device performances. Single pixel GSOI PD revealed similar photoresponse characteristics as well reference GSi PD. The obtained R_{max} of GSOI PD reached 0.52 A/W at the wavelength of 660 nm and the R_{max} of reference GSi PD measured as 0.68 A/W at 905 nm. This result showed that the R_{max} of GSOI shifted towards lower wavelength due to the decrement in the photoactive Si layer with respect to the GSi PD. We also observed the constructive and destructive interference effects due to the multiple reflections within the optical cavities formed between the active Si layer and the BOX layer result in an oscillating behavior of the response mechanism. Subsequently, GSOI PD had the highest detection limit as well as the GSi PD under zero-bias condition. These obtained results clearly guided the photo-detection capability of G/n-Si diode arrays on single substrate using SOI technology.

In section 4.2, we demonstrated that a multi-channel G/n-Si Schottky PDA can be fabricated on SOI substrates using standard microfabrication techniques applied in CMOS technology. In the PDA device structure, monolayer graphene is utilized as a *common* electrode on the four-element n-Si array fabricated with a two-step photolithography process on a single SOI structure. The I–V measurements taken under dark ambient revealed a rectifying Schottky contact between the graphene electrode and each n-Si element in the array. Each of the individual element in the array exhibited a clear photo-response even under self-powered operational mode similar to that observed for the GSOI based single pixel Schottky barrier PD, which was reported in section 4.1. The device parameters, including spectral *R*, specific detectivity, noise equivalent power, and response speed of the GSi PDA sample were systematically investigated in our study. As revealed by wavelength resolved photocurrent spectroscopy measurements, each element in the PDA structure exhibited a maximum spectral *R* of around 0.1 A/W under a self-powered operational mode. Time dependent photocurrent spectroscopy measurements showed an excellent photocurrent reversibility of the device with ~1.36 and ~1.27 μs rise time and fall time, respectively. Each element in the array displayed an average specific detectivity of around $1.3x10^{12}$ Jones and a substantially small noise equivalent power of ~0.14 $pW/Hz^{-1/2}$. This section showed that multiple G/n-Si PDs, operating independently from each other on a single SOI substrate, can be produced simply by employing single layer graphene as the *common* electrode.

In section 4.3, we presented the improvement of SOI based G/n-Si Schottky barrier PDA with *separate* graphene electrode and hence the elimination of optical crosstalk effect occurred between G/n-Si diodes. In this regard, we successfully obtained individual graphene electrodes on arrayed n-Si channels and investigated the optoelectronic characteristics of each diode. All devices exhibited strong rectification behavior and have low leakage current in parallel with high detectivity, low noise and fast operation speed. For instance, G/n-Si diodes showed the highest sensitivity with a maximum spectral response of 0.12 A/W, D^* of 3.5 x 10^{13} Jones and *NEP* of 0.013 pW/Hz$^{-1/2}$ and also devices had a response speed of ~1.32 μs at 660 nm peak wavelength under zero-bias condition. As revealed by optical crosstalk measurement, the *common* and *separate* graphene electrode devices with the same pixel pitch of 1.5 mm had a total crosstalk of about ~0.25 % (-52 dB) and ~0.10% (-60 dB) per array, respectively. Accordingly, disconnected graphene electrodes suppressed the magnitude of the optical crosstalk by a factor of 150 %. These obtained results clearly showed that the optical crosstalk between neighboring n-Si elements can be greatly minimized when graphene is used as separated electrode on arrayed Si on SOI substrate.

In section 4.4, we designed a 2D PDA based on graphene and SOI integration. The integration potential was proposed with a 16 pixel of G/n-Si PDs operated with high sensitivity under zero bias regime. According to the electrical and optoelectronic measurements, each pixel exhibited a clear rectifying Schottky character with low dark current and revealed an excellent photoresponse at R.T. Accordingly, G/n-Si pixel arrays showed an extremely low crosstalk of -61 dB (0.09%) between neighboring pixels when compared with the crosstalk results of the state-of-art Si based lateral interdigitated p-i-n PDs. We also simulated this novel device as a passive matrix array for use in image sensing applications. Therefore, the variation in V_{OC} and I_{SC} for each of the pixels was also systematically compared each other. In this regard, pixel with three different photo-detection capability was correlated with the surface coverage of graphene sheet by micro-Raman mapping of 2D peak. We observed that a homogeneous coverage of the graphene throughout the active junction area has an impact of the photosensitive pixel quality. Due to the inhomogeneities at the G/n-Si interface, the optoelectronic properties of the device differed from pixel to pixel and altered the on/off performance of PDs. For the future work, our proof-of-concept study may be developed for higher contrast and resolution of M by N image sensors to be used in our daily life with the integration of graphene and SOI technology.

To summarize briefly, we suppressed the optical crosstalk effect in our device structure as following; (i) using n-Si substrate with a similar doping level of graphene (unintentionally p-type doped with an intrinsic hole carrier concentration of about 10^{13} cm^{-2}), (ii) aligning the array geometry including the PD size and pitch of the detector array on SOI substrate and (iii) arranging the absorption layer as ~1 μm in zero-bias condition. Moreover, these obtained experimental findings guided that the SOI based self-powered 1-D PDA and 2-D PDA devices showed considerable suppression in terms of magnitude optical crosstalk compared to InGaAs, Si and Ge based p-i-n PDA counterparts that need external bias. Conversely, the magnitude of optical crosstalk measured for devices with *separate* graphene electrode is even better than *common* electrode one which requires fewer lithography steps in fabrication route. This thesis may offer exciting opportunities for the realization of high-value added technological applications based on motion and position detection, imaging, and spectrophotometry in which graphene and SOI technology can be used together.

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PUBLICATIONS

A. Yanilmaz, Ö. Ünverdi, C. Çelebi
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